

PCIe Gen-5 U.2 Test Adapters

Performance Report



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High-Speed Serial Results

The high-speed serial measurements of the PCIe Gen5 U.2 adapters use a 4-port (50-ohm) VNA calibrated from 50MHz to 40GHz with 800 points. The measurements are in the form of s-parameters.

The s-parameter measurements are renormalized to 42.5-ohm ports instead of 50-ohm ports. This was done so that the port impedance and adapter impedance match.

In addition, 2.92mm to MMPX adapters and MMPX connectors are included in the s-parameter measurements, but they are then gated out of the return loss due to their 50-ohm impedance.

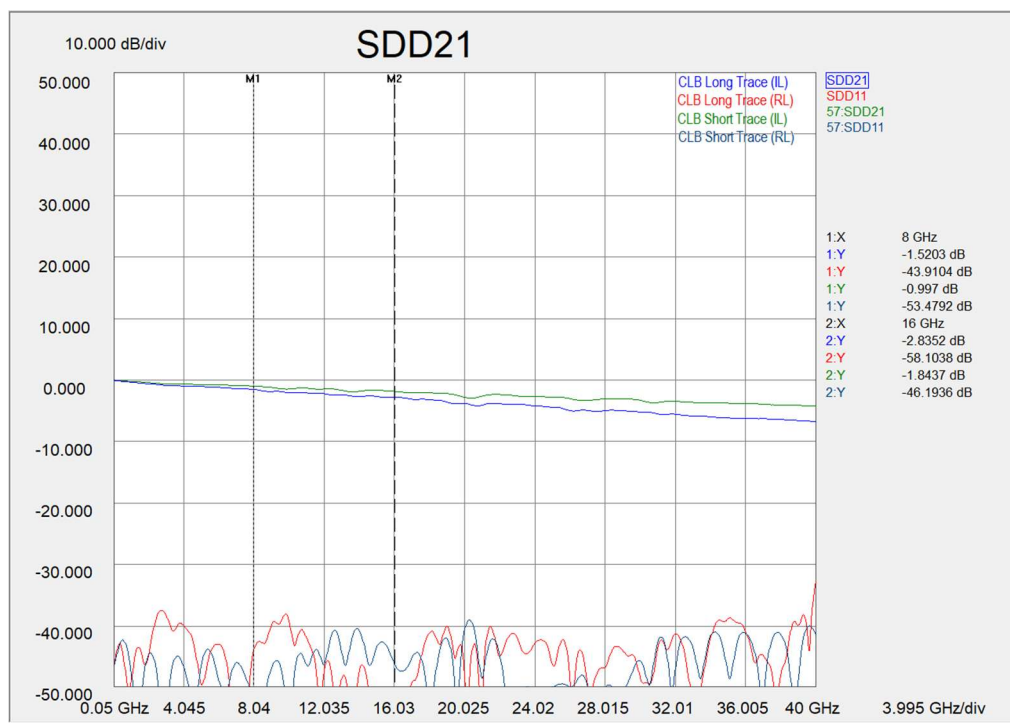
Ultimately, this post-processing makes the s-parameters accurately represent the performance of the high-speed channels of only the U.2 adapters.

Characterization (CLB and CBB Independent Only):

To characterize the real high-speed channels of the adapters only (no connector), the replica channels must be used. These replica channels include MMPX connector lead-in for what would be the U.2 connector side of the high-speed channels. This MMPX connector lead-in that is part of the S-parameter measurement must then be de-embedded to represent the real high-speed channels.

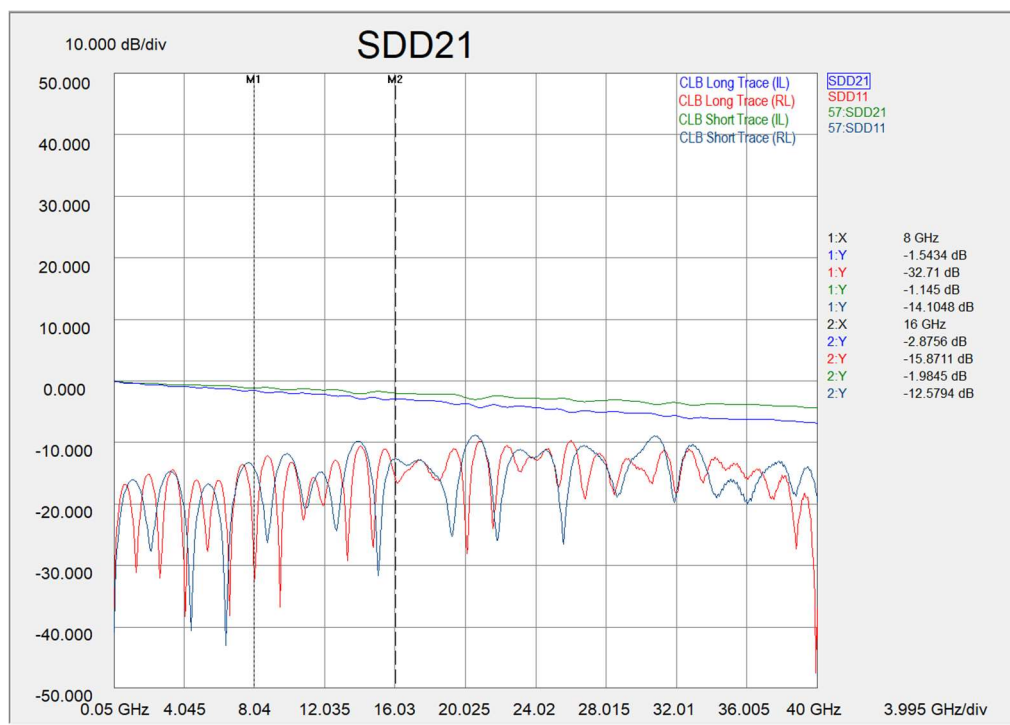
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Figure 1: CLB Only Characterization



Corrected return loss maintains below -30dB.

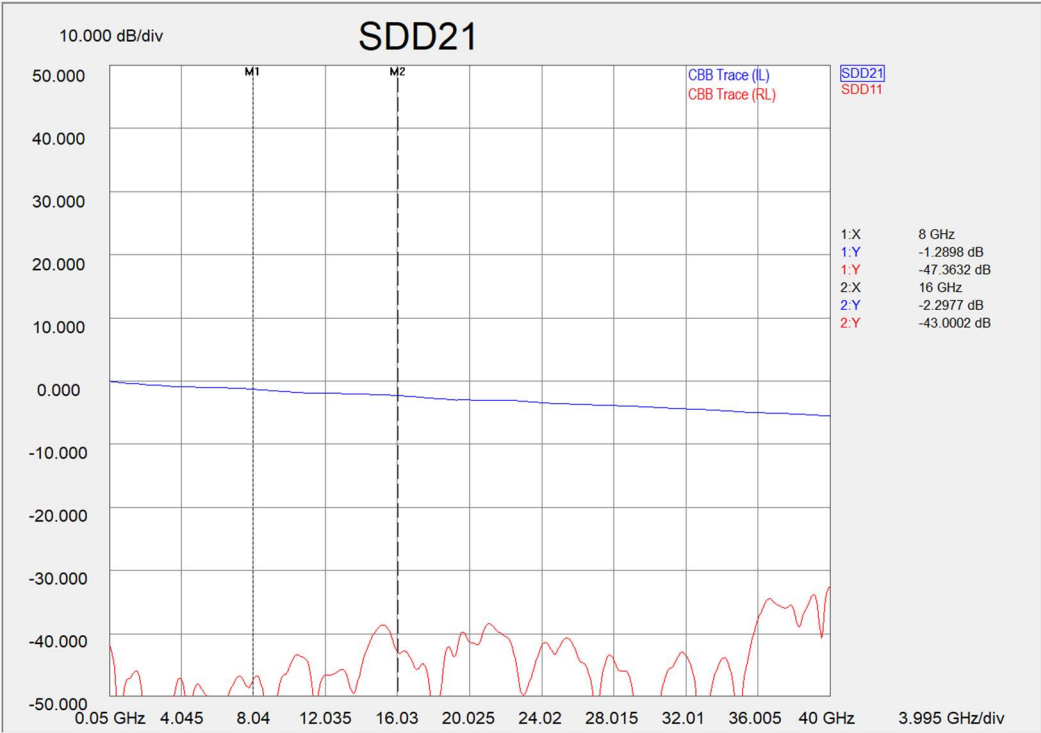
Figure 2: CLB Only Characterization, No Normalization or Gating



Uncorrected return loss maintains below -8dB.

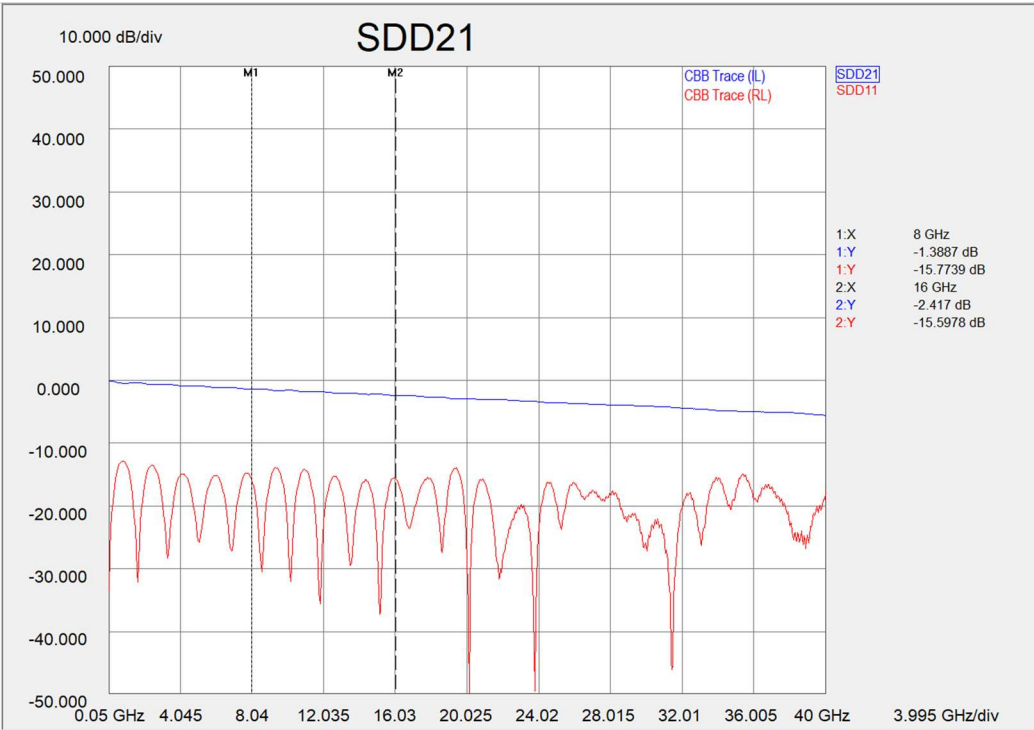
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Figure 3: CBB Only Characterization



Corrected return loss maintains below -30dB.

Figure 4: CBB Only Characterization, No Normalization or Gating

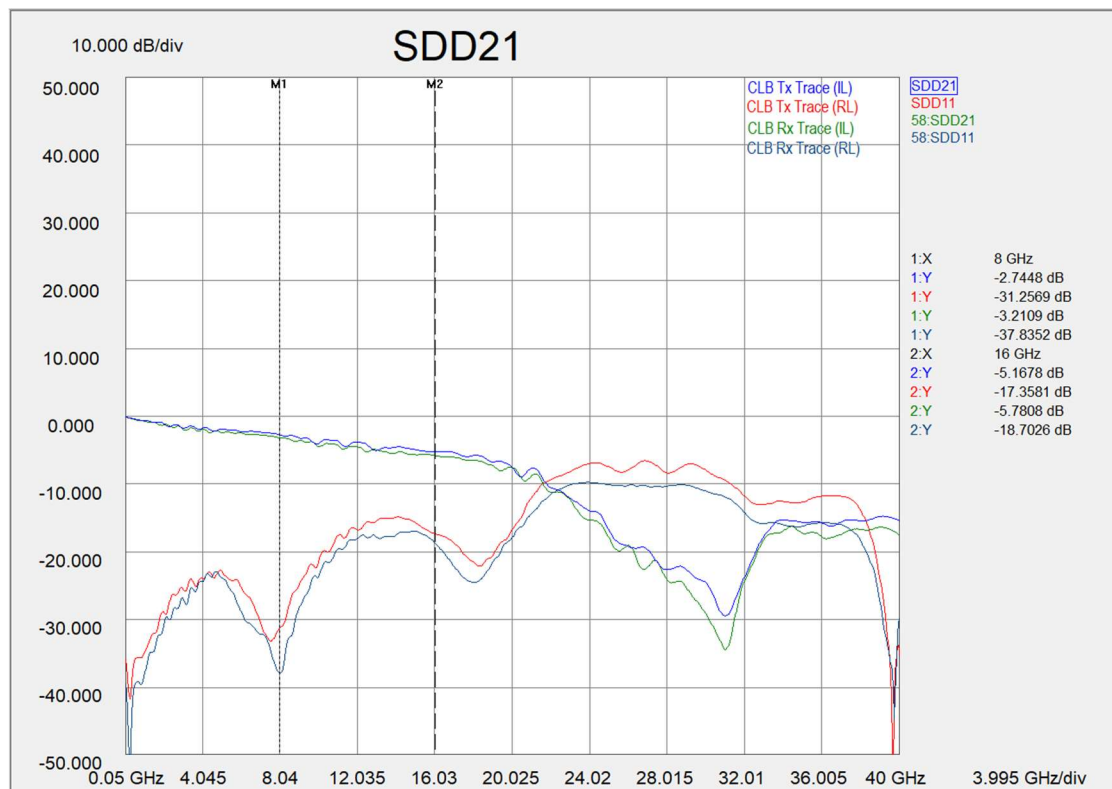


Uncorrected return loss maintains below -10dB.

Mated CLB/CBB (CLB and CBB Independent Only):

These s-parameter measurements are made when the CLB and CBB are mated. The U.2 connector is included in the measurement. The MMPX connectors and 2.92mm to MMPX adapters are included in the s-parameter, but then are gated out.

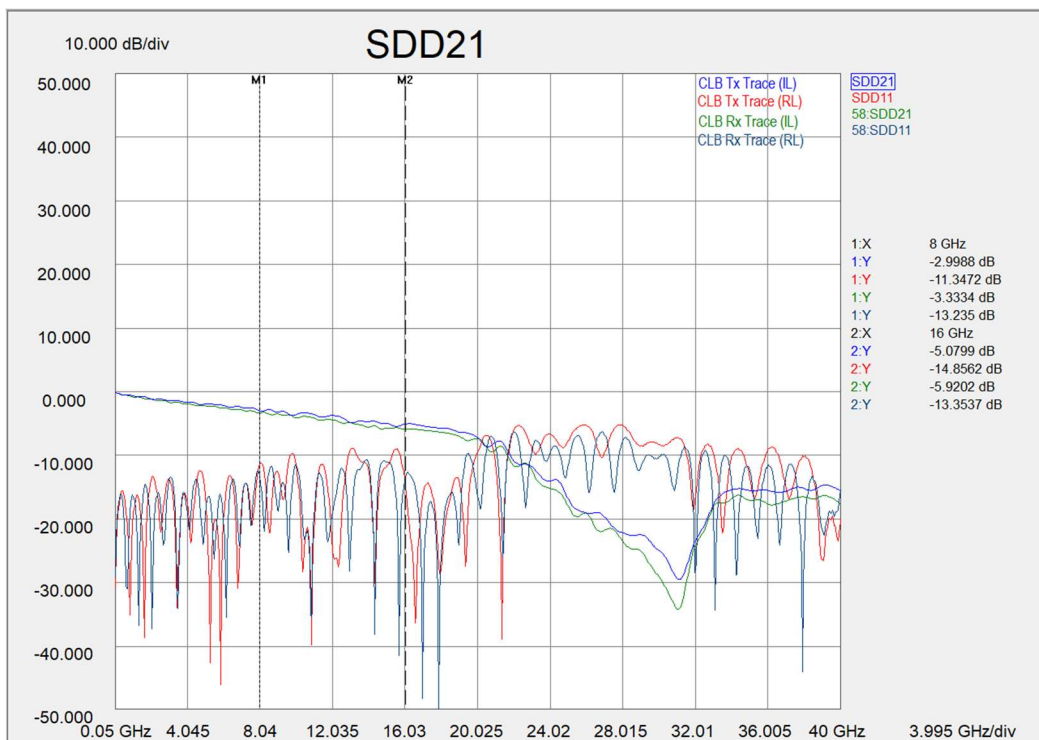
Figure 5: CLB and CBB Mated Insertion and Return Loss



Return Loss is near or below -5dB from 10MHz to 40GHz. There are no significant resonances.

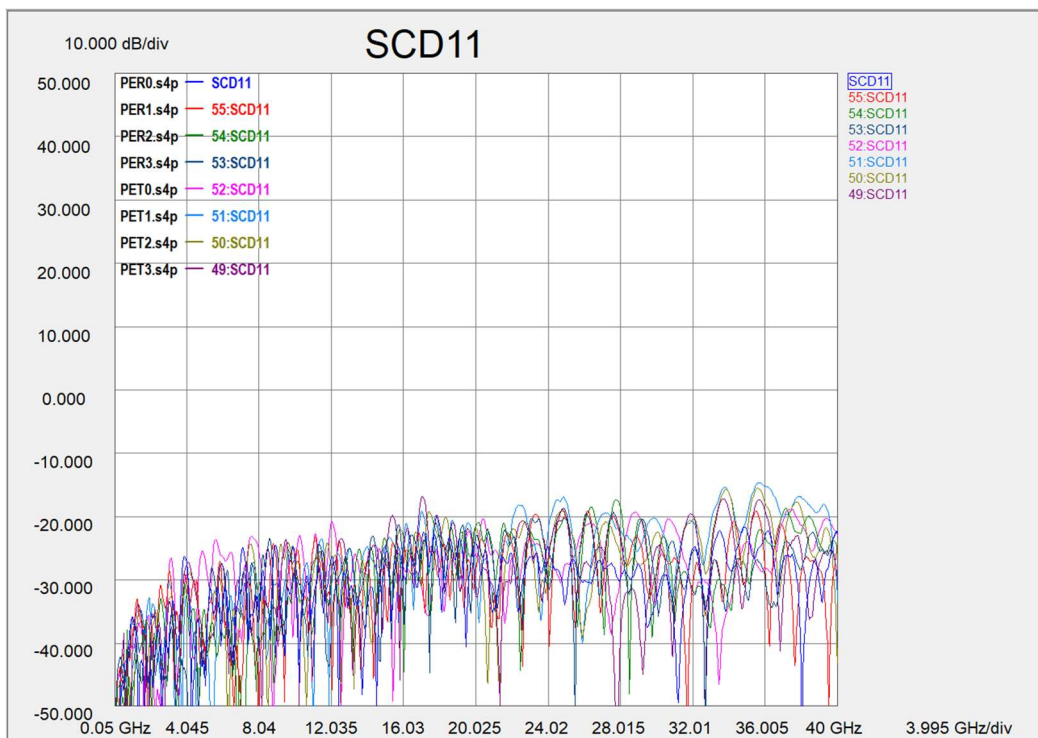
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Figure 6: CLB and CBB Mated Insertion and Return Loss, No Normalization or Gating



Uncorrected return loss maintains below -5dB.

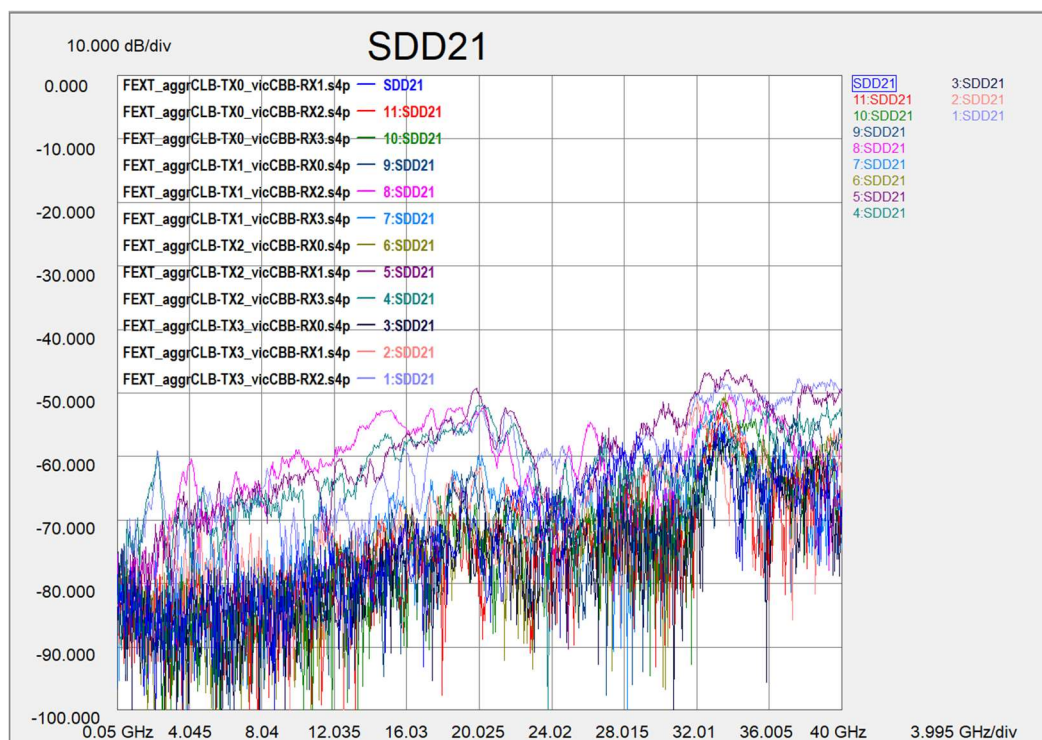
Figure 7: CLB and CBB Mated Conversion Loss



Maintains below -15dB for all frequencies except after 32GHz.

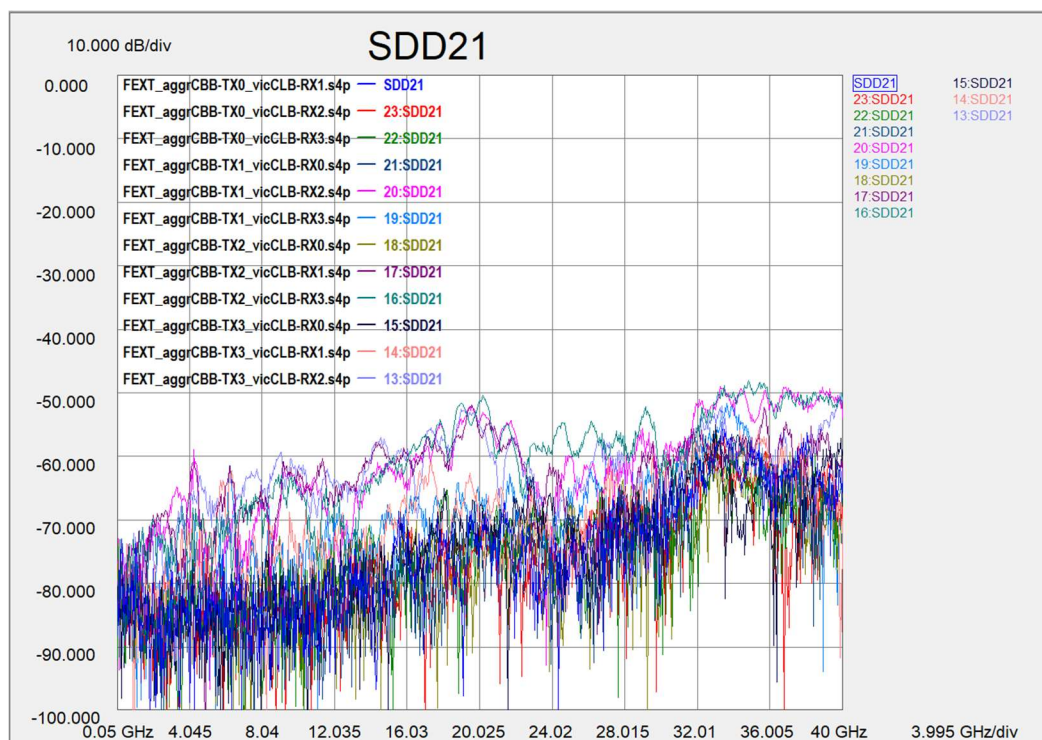
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Figure 8: CLB and CBB Mated FEXT



Maintains at or below -50dB for all frequencies except after 32GHz.

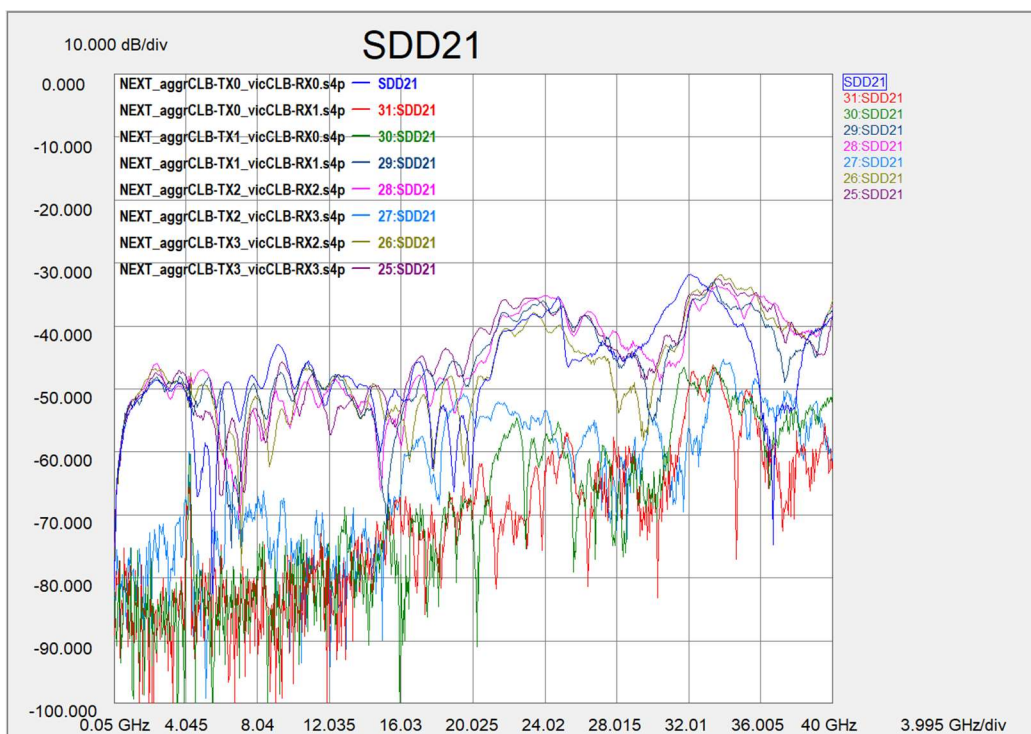
Figure 9: CBB and CLB Mated FEXT



Maintains at or below -50dB for all frequencies except after 32GHz.

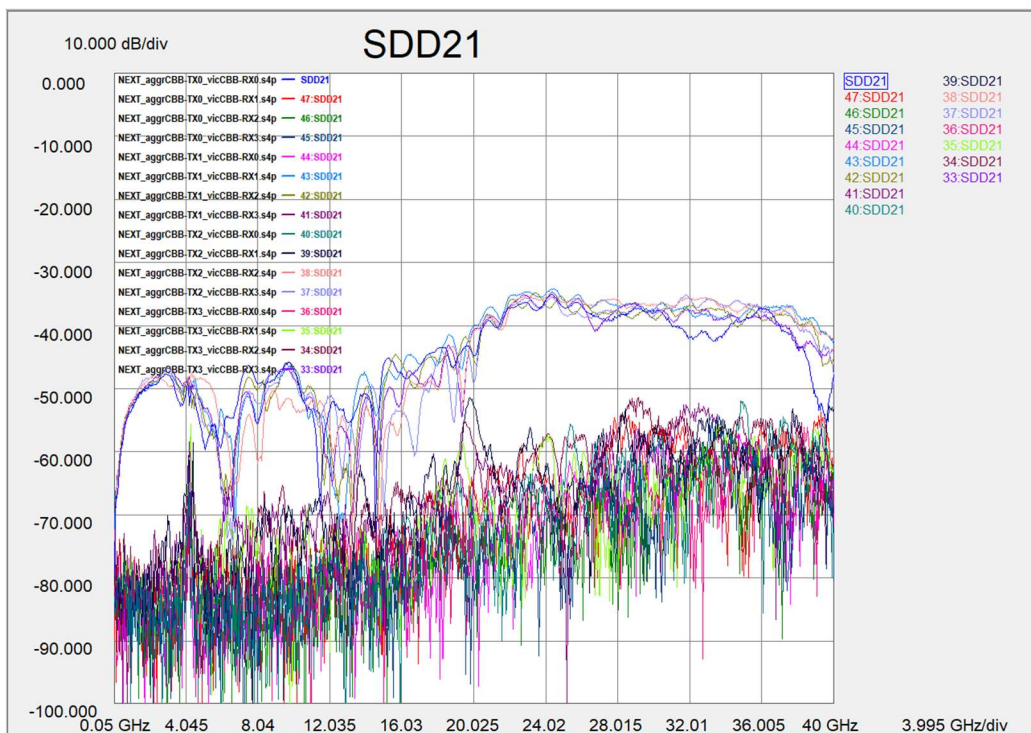
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Figure 10: CLB Mated NEXT



Maintains at or below -30dB for all frequencies.

Figure 11: CBB Mated NEXT



Maintains at or below -33dB for all frequencies.

Fixture Test Channel Setup:

Figure 12: Total Test Channel Loss for Gen5

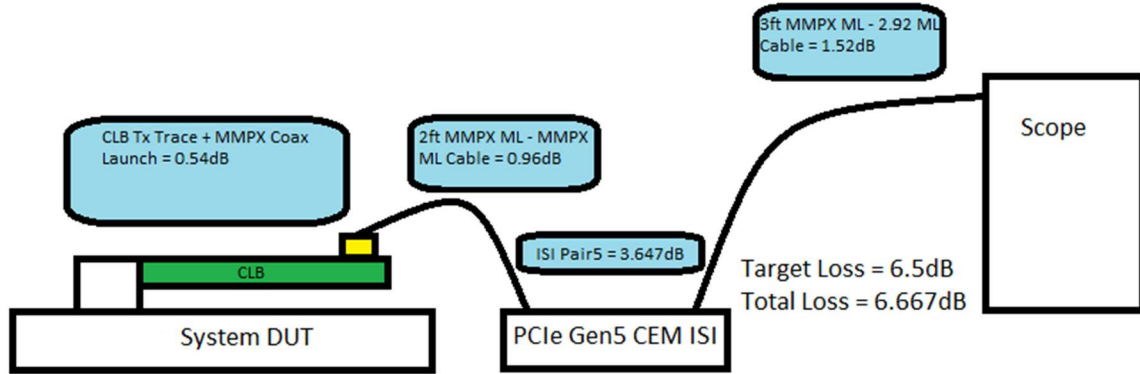


Figure 13: Total Test Channel Loss for Gen4

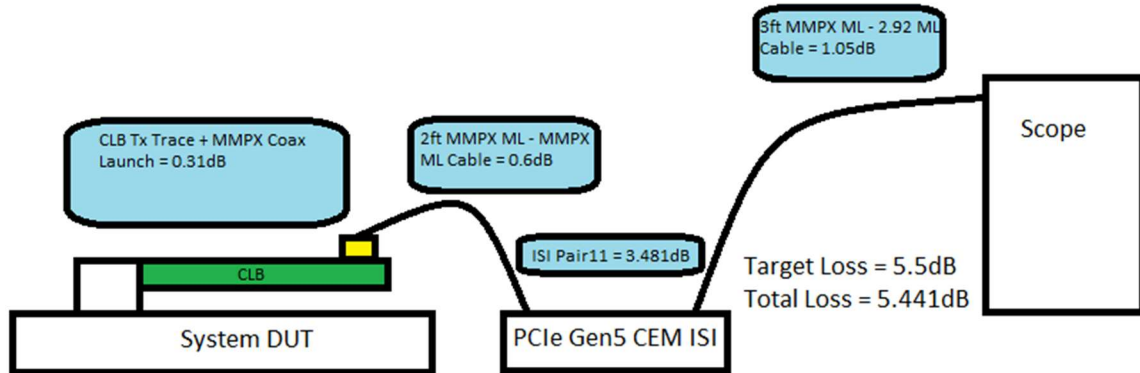
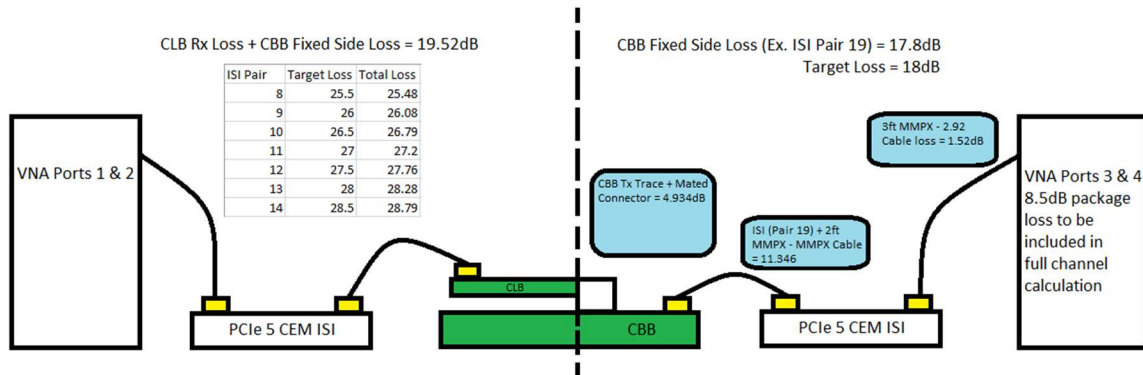
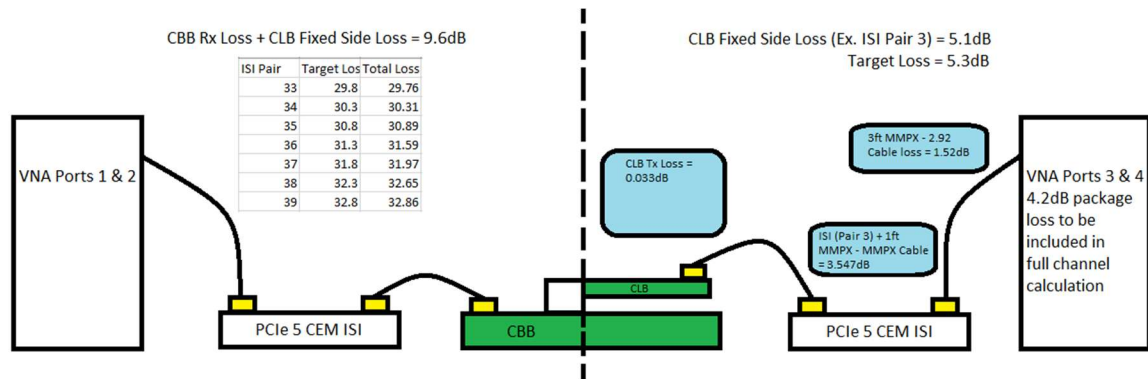


Figure 14: System Rx Calibration Example



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Figure 15: AIC Rx Calibration Example



Voltage Rail Results

Loading:

An electronic load is connected to each voltage rail one at a time with the load according to the current values in the figure from the U.2 specification shown below.

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Figure 16: Table 4-1 from PCI Express U.2 Specification

Table 4-1. Power Supply Rail Requirements

Parameter	Description	Value
P_{max}	Maximum sustained power ⁴	30 W (max) ⁸
$P_{init-limit}$	Initial slot power limit ⁴	25 W (max)
+12 V _{tol}	Voltage tolerance (at pin) ⁵	-
+12 V _{amp}	Max continuous current ¹	2.45 A (max) ⁷
+12 V _{peak-amp}	Max peak current ²	4.5 A (max)
+12 V _{ramp-amp}	Max power-up ramp current ³	2 A (max)
+12 V _{drop}	Voltage drop across connector	80 mV (max)
+3.3 V _{Auxtol}	Voltage tolerance (at pin)	±15 % (max)
+3.3 V _{Auxamp}	Max continuous current ¹	1 mA (SMBus inactive) 5 mA (SMBus or +12 V active)
+3.3 V _{Auxcap}	Max cap load ⁶	5 µF (max)
SMBus delay	Delay from +3.3 Vaux power valid to SMBus ready	500 ms (max)
	Delay from +12 V power valid to vital product data available.	500 ms (max)
	Delay from PERST# de-assertion (optional) to SMBus ready	500 ms (max)

Notes:

- Maximum continuous current is defined as the highest averaged current value over any one second period.
- Maximum current, to limit connector damage and instantaneous power.
- Maximum current load presented by the SFF-8639 module on the power rail of the SFF-8639 receptacle during the initial power-up ramp to 90% of the minimum SFF-8639 module operating voltage.
- For devices that are capable of consuming more than the Initial slot power limit, the Slot Power Limit Support functionality is used to configure a higher maximum limit. The Slot Capabilities register is defined in the *PCI Express Base Specification*. Devices may negotiate an operational power limit equal to or less than the PCIe configured Slot Power Limit using mechanisms outside the scope of this specification.
- Vendor specific. No tolerance specified.
- Maximum capacitance presented by the SFF-8639 module on the power rail at the SFF-8639 receptacle.
- The maximum value represents the allowed maximum current at the maximum power and the minimum voltage.
- Based on SFF-8639 connector current limit multiplied by minimum input voltage.

Figure 17: Electronic Load Results for the 12V Rail

E-Load (Amps)	Voltage at E-Load (Volts)	DMM Measurement at CLB Connector (Volts)	DMM Measurement at CBB Connector (Volts)	Drop through connector (Volts)
No Load	12.4550	12.46	12.47	0.01
0.1A	12.4243	12.43	12.43	<0.01
0.2A	12.4109	12.42	12.42	<0.01
0.3A	12.4011	12.41	12.41	<0.01
0.4A	12.3839	12.4	12.4	<0.01
0.5A	12.3633	12.38	12.38	<0.01
0.75A	12.3081	12.32	12.33	0.01
1.0A	12.2545	12.27	12.29	0.02
1.5A	12.1678	12.2	12.21	0.01
1.75A	12.1416	12.17	12.19	0.02
2.0A	12.1260	12.16	12.18	0.02
2.45A	12.1000	12.14	12.17	0.03

The voltage is within the tolerance at the CBB test points. The voltage rails are successfully loaded with no unexpected voltage drops and no overheating.

REFCLK Results (CBB Independent Only)

A differential probe along with 2.92mm to MMPX cables were used to measure the REFCLK waveform generated by the CBB independent adapter on the oscilloscope.

This waveform was then saved to a .bin file and imported into the Clock Jitter Tool.

PCI-SIG website provided a link to this test tool.

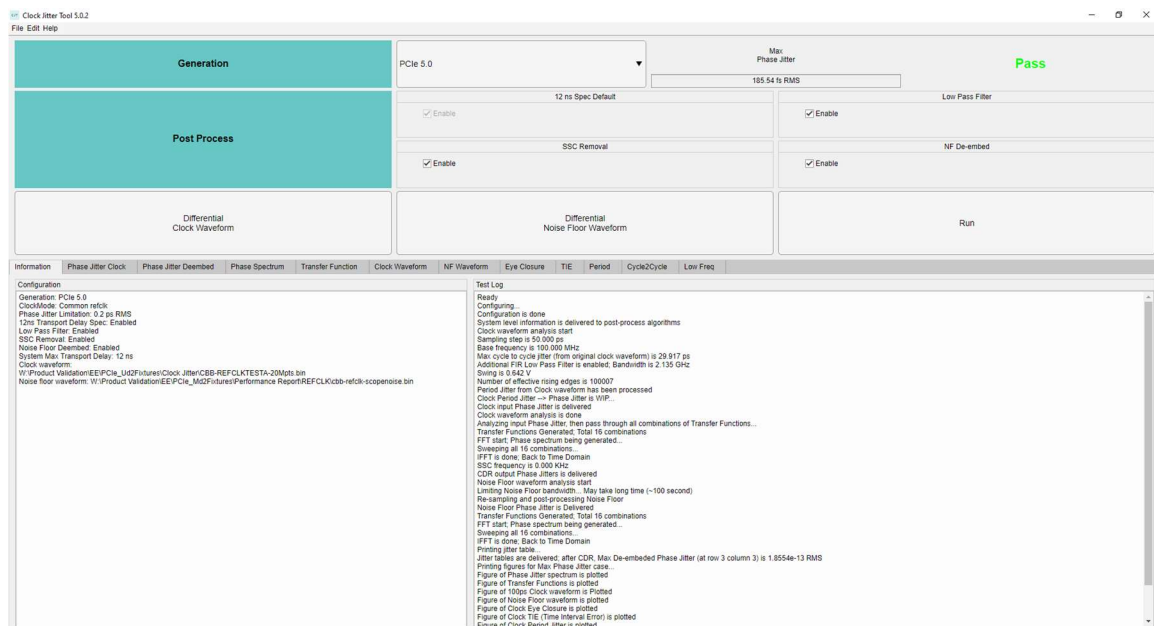
Jitter A:

REKCLK A passes phase jitter requirements.

The max phase jitter shows 185.54 fs RMS which is below 200fs RMS limit in the PCIe specification.

Note: Real Time Scope noise has been removed during post processing.

Figure 18: Clock Jitter A Tool Results Window



Jitter B:

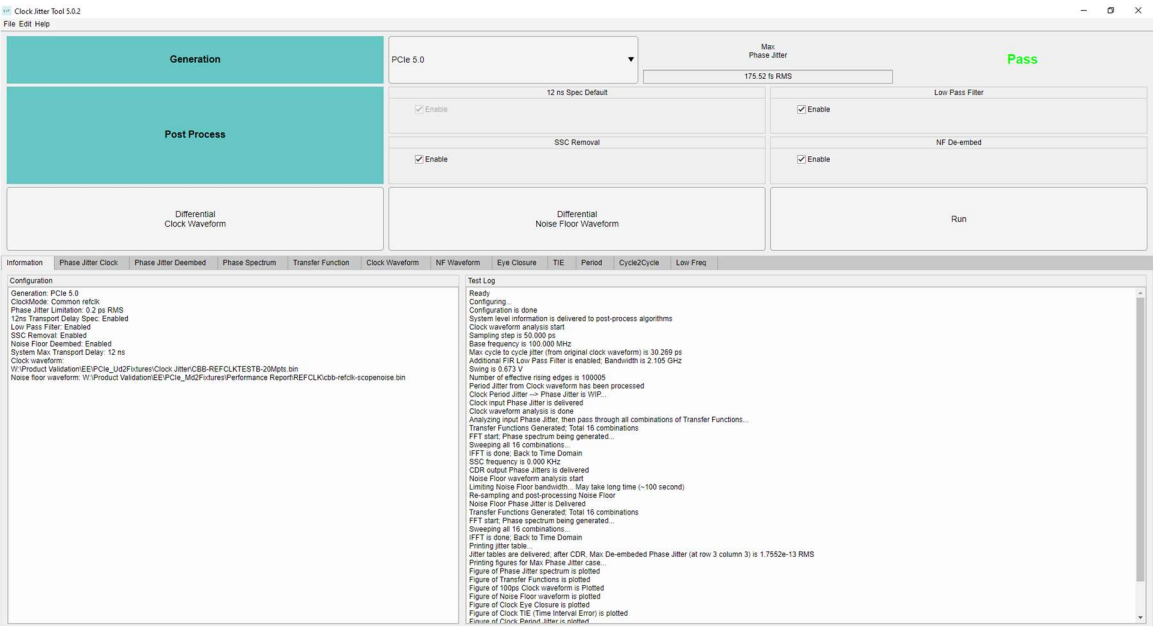
REKCLK B passes phase jitter requirements.

The max phase jitter shows 175.52 fs RMS which is below 200fs RMS limit in the PCIe specification.

Note: Real Time Scope noise has been removed during post processing.

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Figure 19: Clock Jitter B Tool Results Window



Characteristics:

Period: 9.9990021ns, Pass

V max/mind: +/-353mV, Pass

Rise time: 656ps, Rise Time Rate: 0.79V/ns, Pass

Fall time: 654ps, Fall Time Rate: 0.86V/ns, Pass

Figure 20: REFCLKA Characteristics on Real Time Oscilloscope



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Characteristics:

Period: 9.9996526ns, Pass

V max/mind: +/-367mV, Pass

Rise time: 653ps, Rise Time Rate: 0.74V/ns, Pass

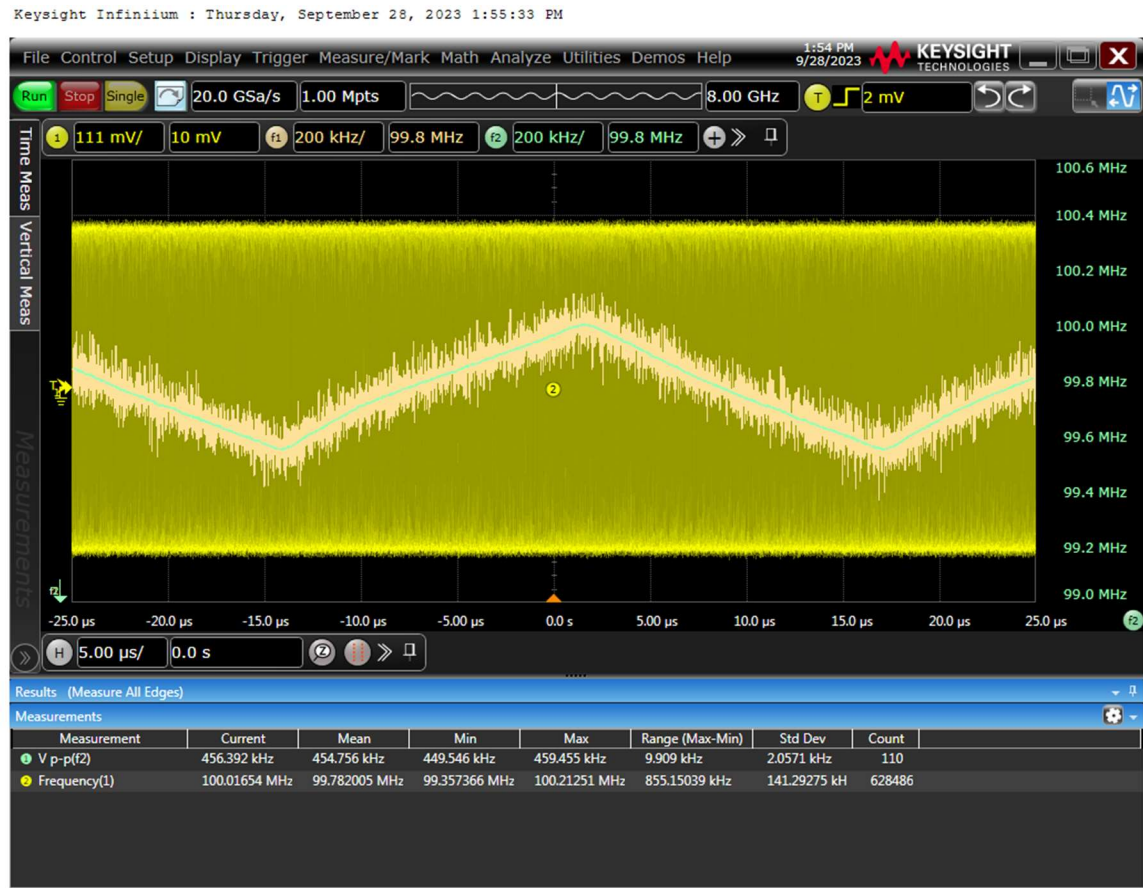
Fall time: 647ps, Fall Time Rate: 0.81V/ns, Pass

Figure 21: REFCLKB Characteristics on Real Time Oscilloscope



SSC:

Figure 22: REFCLKA with SSC set at -0.5% down spreading



SSC Setting: -0.5%, Actual -0.46%

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Figure 23: REFCLKB with SSC set at -0.5% down spreading



SSC Setting: -0.50%, Actual -0.46%

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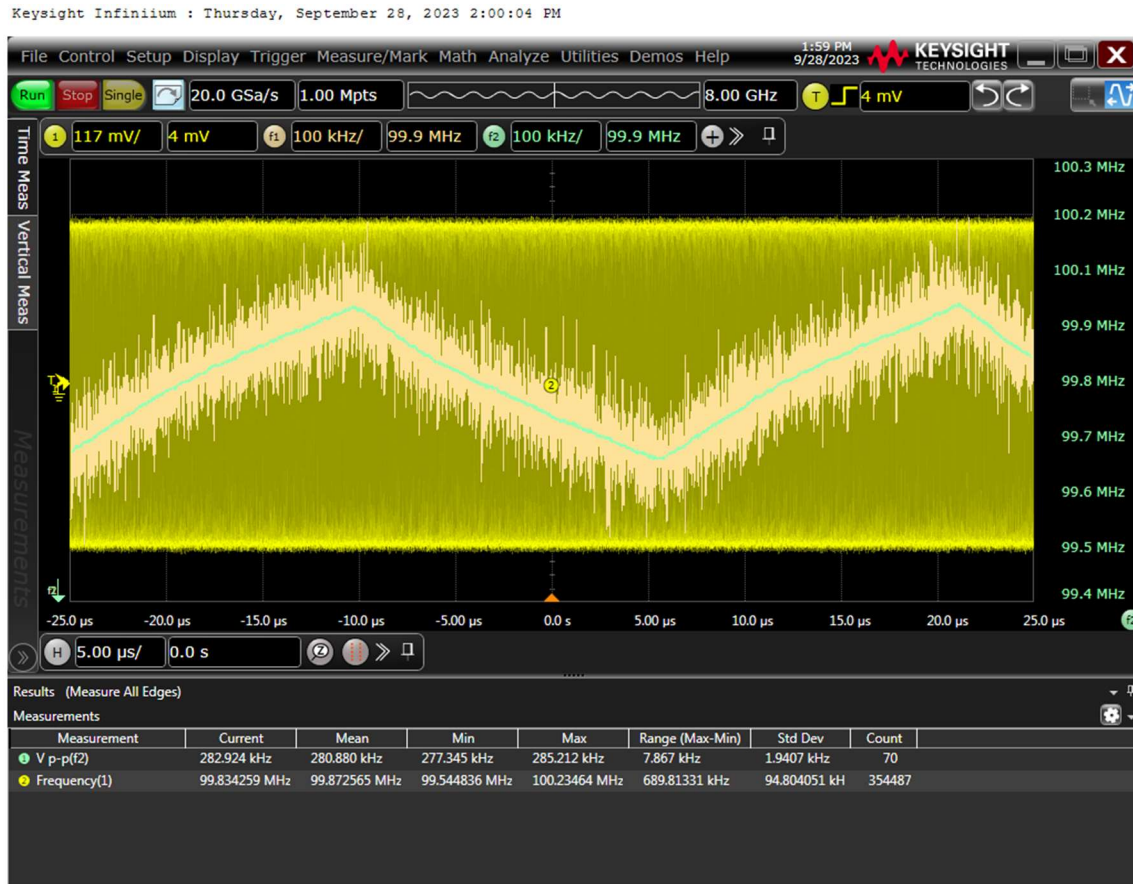
Figure 24: REFCLKA with SSC set at -0.25% down spreading



SSC Setting: -0.25%, Actual -0.28%

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Figure 25: REFCLKB with SSC set at -0.25% down spreading



SSC Setting: -0.25%, Actual -0.28%

CMTS (Compliance Mode Toggle Signal) Results

A differential probe along with 2.92mm to MMPX cables were used to measure the CMTS waveform and equalization presets on the oscilloscope. CMTS push button was used to activate the CMTS.

Characteristics:

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Figure 26: 40mV Noise Test of CMTS



The noise is under +/-40mV before and after the trigger of CMTS.

Figure 27: CMTS Frequency



The CMTS frequency shows a mean of 99.989021MHz.

Figure 28: CMTS Pulse Length



The CMTS time length is 1ms.

These characteristics are adequate for toggling transmitter equalization presets.

PERST Results

This PERST test is accomplished using an oscilloscope with header connection probes. They connect at the 1.8V rail test point and the PERSTn trace on the CBB.

The voltage rail and PERSTn transition can be seen on the oscilloscope on CBB start-up. The PERSTn transition can also be seen when the PERST button is pressed on the CBB. The delay between these transitions is then measured on the oscilloscope.

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Automatic (Start-Up):

Designed delay = 100ms

Measured delay = 101.11ms

The figure below shows the delay between the 1.8V rail and PERSTn signal.

Figure 29: Delay Measurement between 1.8V rail start-up and PERSTnA Rise on Real-Time Oscilloscope



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Automatic (Start-Up):

Designed delay = 100ms

Measured delay = 104.44ms

The figure below shows the delay between the 1.8V rail and PERSTn signal.

Figure 30: Delay Measurement between 1.8V rail start-up and PERSTnB Rise on Real-Time Oscilloscope



Manual (Push-Button Activated):

Designed delay = 100ms

Measured delay = 102.78ms

The figure below shows the delay between the PERST button push and PERSTn signal.

Figure 31: Delay Measurement After PERSTA Button Press on Real-Time Oscilloscope



Manual (Push-Button Activated):

Designed delay = 100ms

Measured delay = 104.44ms

The figure below shows the delay between the PERST button push and PERSTn signal.

Figure 32: Delay Measurement After PERSTB Button Press on Real-Time Oscilloscope





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©2024 Wilder Technologies, LLC
Document No. 910-0078-100 Rev. B
Initial Release: 2/22/23
Updated: 2/29/24