# PCIe Gen-5 U.2 Test Adapters

User Manual

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# Introduction

This user's guide documents the PCIe Gen-5 U.2 Test Adapters. The Test Adapters shown in Figure 1, tests PCIe Gen-5 U.2 hosts and devices against the PCIe Specification. The model numbers for the PCIe Gen-5 U.2 Test Adapters are as follows:

**Table 1. Available Models**

| MODEL NUMBERS | DESCRIPTION |
|---|---|
| PCIEG5-U2-TPA-CLB | CLB + CMTS + Accessories |
| PCIEG5-U2-TPA-CBB | CBB + CMTS + Accessories |
| PCIEG5-U2-TPA-CLBCBB | CLB + CBB + CMTS (2x) + Accessories |
| PCIEG5-U2-TPA-CLBCBB-DPT | CLB + CBB + CMTS (4x) + Accessories |
| PCIE-CMTS-TPA | CMTS |

The CLB and CBB Test Adapters fixtures allow easy access, via high-speed MMPX connections, to measure or inject data signals.

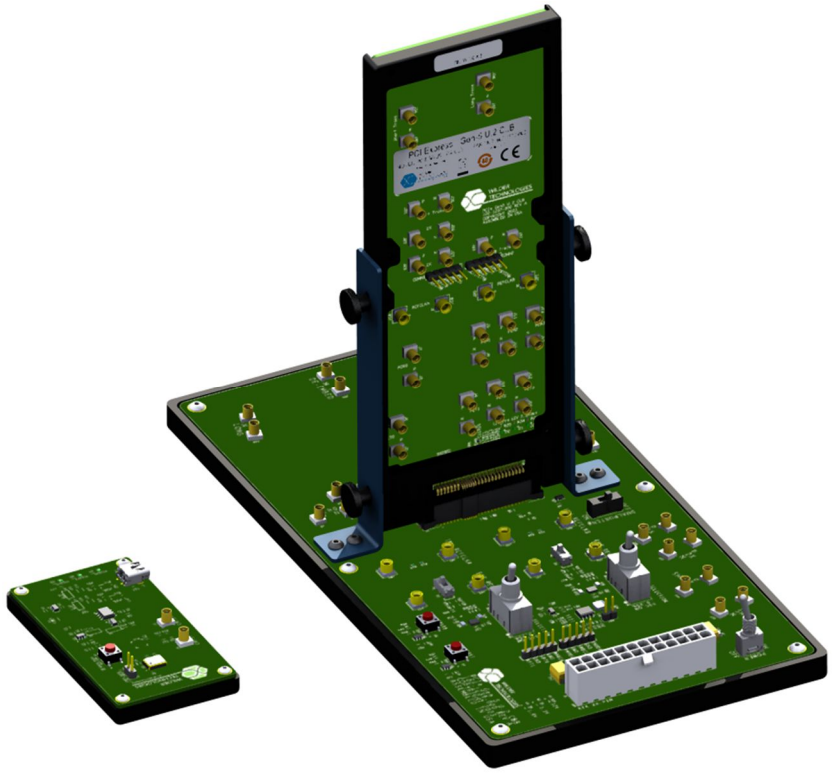

Figure 1. PCIe Gen-5 U.2 Test Adapters

# PCIe Gen-5 U.2 Accessories and Optional Accessories

## PCIe Gen-5 U.2 Accessories

The PCIEG5-U2-TPA Test Adapters are provided with the following materials in Figure 2 that allow the user to properly interface with the fixtures and/or DUT. The power supply and power cord are only included with the PCIEG5-U2-TPA-CBB for power. A 2.92mm female to SMP female 9” cable assembly pair is included with each PCIEG5-U2-TPA-CBB and PCIEG5-U2-TPA-CLB model. Lastly, one Wilder CMTS Interface 12” cable assembly pair is included with each PCIE-CMTS-TPA model, exclusively to be used as a CMTS interface cable only.

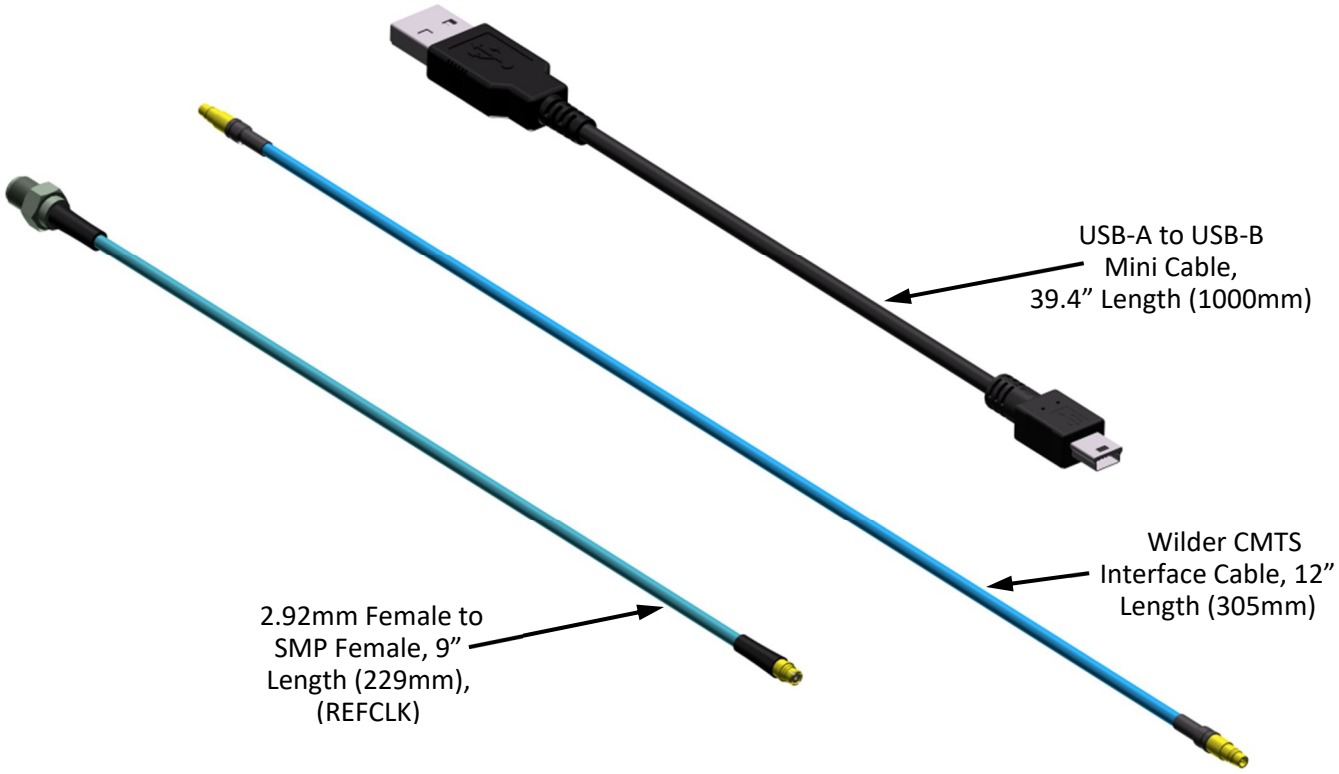


Figure 2. The PCIe Gen-5 U.2 included accessories (NOT modeled to scale)

## PCIe Gen-5 U.2 Optional Accessories

There are numerous Huber+Suhner PCIe Gen-5 accessories, such as adapters or cable assemblies, available for purchase from Richardson RFPD. The table below indicates the Huber+Suhner part numbers for the optional accessories.

**Table 2. Optional PCIe Gen-5 Accessories from Richardson RFPD**

| HUBER+SUHNER PART NUMBER | HUBER+SUHNER DESCRIPTION | DETAILS |
|---|---|---|
| 84071648 | 33MMPX-SK-50-1E | RF Adapter – Between series MMPX Male to SK (2.92 mm) Female |
| 84071696 | 33SK-MMPX-50-1E | RF Adapter – Between series SK Male to MMPX Female |
| 80351638 | 024E573HTCR092HTCR2.5PM1PS-STD | RF Cable – SMP Female to SMA Female, 2.5” Long (63.5 mm) |
| 85105115 | PCI SF102E/11SK/11SK/914mm | RF Cable – SK Male to SK Male, 36” Long (914 mm) |
| 85108590 | PMA SF102E/11MMPX/11MMPX/305mm | RF Cable – MMPX Male to MMPX Male, 12” Long (305 mm) |
| 85119609 | 024E430CR092KCR4PM1PS-STD | RF Cable – MMPX Male to SK Female, 4” Long (102 mm) |
| 85152826 | PCI SF102E/11MMPX/11SK/914mm | RF Cable – MMPX Male to SK Male, 36” Long (914 mm) |
| 85174413 | PCI 65_MMPX Kit | MMPX 50-Ohm Terminator Kit |

**NOTE: To avoid damaging attaching cables or the test adapters, use the handling techniques described in the Care and Handling section before making any connections or configuring a test setup.**

**Always use a static-safe workstation when performing tests, as explained in the "Electrostatic Discharge Information" section.**

## Product Inspection

Upon receiving the PCIe Gen-5 U.2 Test Adapters from Wilder Technologies, perform the following product inspection:

- Inspect the outer shipping container, foam-lined instrument case, and product for damage. Retain the outer cardboard shipping container until the contents of the shipment have been inspected for completeness and the product has been checked mechanically and electrically. Use the foam-lined instrument-case for secure storage of the Wilder Technologies PCIe Gen-5 U.2 Test Adapters when not in use.

- Locate the shipping list and verify that all items ordered were received.

- In the unlikely event that the product is defective or incomplete, the "Limited Warranty" (see the Wilder web site) discusses how to contact Wilder Technologies for technical assistance and/or how to package the product for return.

# The PCIe Gen-5 U.2 Test Adapters and Handling Precautions

The PCIe Gen-5 U.2 Test Adapters require careful handling to avoid damage. Improper handling techniques, or using too small of a cable bend radius, can damage the coaxial cable connections. This can occur at any point along the cable. To achieve optimum performance and to prolong the PCIEG5-U2-TPA Test Adapters' life, observe the following handling precautions:

- **CAUTION 1: Avoid Torque Forces** (Twisting)
  While individual coaxial cables mating to the fixture may have some rotational freedom, twisting the fixture as a unit, with one end held stationary, may damage, or severely degrade performance. Adherence to Caution 5 (below) helps to avoid twisting.

- **CAUTION 2: Avoid Sharp Cable Bends**
  Never bend coaxial cables into a radius of 26 mm (1-inch) or less. Never bend cables greater than 90°. Single or multiple cable bends must be kept within this limit. Bending mated cables to the fixture less than a 26mm (1-Inch) radius will permanently damage or severely degrade overall performance.

- **CAUTION 3: Avoid Cable Tension** (Pull Forces)
  Never apply tension (pull forces) to an individual coaxial cable that is greater than 2.3 kg (5 lbs.). To avoid applying tension, always place accessories and equipment on a surface that allows adjustment to eliminate tension on the cables. Use adjustable elevation stands or apparatus to accurately place and support the fixture.

  If the test set-up requires repositioning, first loosen, or disconnect the cable connections to avoid twisting, bending, or tension.

- **CAUTION 4: Independently Support Instrument Cables or Accessories**
  Excessive weight from instrument cables and/or accessories connected to the test fixtures can cause damage or affect the test fixture's performance. Be sure to provide appropriate means to support and stabilize all test set-up components.

# General Test Adapters, Cable, and Connector

Observing simple precautions can ensure accurate and reliable measurements.

## Handling and Storage

Before each use of the PCIEG5-U2-TPA test fixtures, ensure that all connectors are clean. Handle all cables carefully and store the test fixtures in the foam-lined instrument case when not in use, if possible. Do not set connectors contact end down. Install the MMPX protective end caps when the test fixtures are not in use.

## Visual Inspection

Be sure to inspect all cables and MMPX connectors carefully before making a connection. Inspect all cables for metal particles, scratches, deformed threads, dents, or bent, broken, or misaligned center conductors. Do not use damaged cables.

## Cleaning

If necessary, clean the connectors using low-pressure (less than 60 PSI) compressed air or nitrogen with an effective oil-vapor filter and condensation trap. Clean the cable threads, if necessary, using a lint-free swab or cleaning cloth moistened with isopropyl alcohol. Always completely dry the connector before use. Do not use abrasives to clean the connectors. Re-inspect connectors, making sure no particles or residue remains.

## Making Connections

Before making any connections, review the “Care and Handling Precautions**”** section. Follow these guidelines when making connections:

- Align cables carefully
- Make preliminary connection lightly
- To tighten, turn connector nut only
- Do not apply bending force to cable
- Do not over-tighten preliminary connections
- Do not twist or screw-in cables
- Use an appropriately sized torque wrench, and do not tighten past the “break” point of the torque wrench (normally set to 5-inch pounds)

# Electrostatic Discharge Information

Protection against electrostatic discharge (ESD) is essential while connecting, inspecting, or cleaning the PCIEG5-U2-TPA test adapters and connectors attached to a static-sensitive circuit (such as those found in test set).

Electrostatic discharge can damage or destroy electronic components. Be sure to perform all work on electronic assemblies at a static-safe workstation, using two types of ESD protection:

- Conductive table-mat and wrist-strap combination
- Conductive floor-mat and heel-strap combination

When used together, both types provide a significant level of ESD protection. Used alone, the table-mat and wrist-strap combination provide adequate ESD protection. To ensure user safety, the static-safe accessories must provide at least 1 MΩ of isolation from ground. Acceptable ESD accessories may be purchased from a local supplier.

**WARNING: These techniques for a static-safe workstation should not be used when working on circuitry with a voltage potential greater than 500 volts.**

# User Models

The PCIEG5-U2-TPA test adapters support electrical testing of the PCIe Specification. It can perform well beyond the scope of measurements required, limited only by the specifications, environmental, care and handling as stated in this document.

**Note:** The PCIe Gen-5 CEM Variable ISI board (PCIe-VAR-ISI) is required for achieving total channel loss of TX test setup as well as system RX and device RX calibrations. Other accessories required for validation can be purchased from Richardson RFPD (refer to the PCIe Gen-5 U.2 Optional Accessories section).

## CMTS Board Features

The standalone CMTS (Compliance Mode Toggle Signal) board generates a 1 ms pulse with a frequency of 100 MHz to cycle through compliance presets. The CMTS board has the following features.


Figure 3. CMTS Pulse Duration (1 ms)


Figure 4. CMTS Frequency (100 MHz)

USB Mini-B connector to provide power to CMTS board.

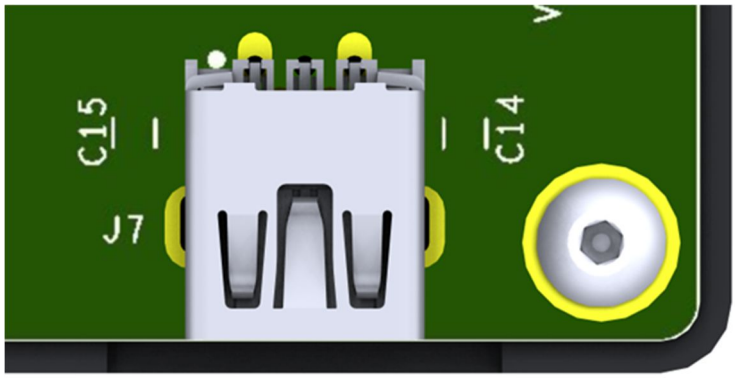


Figure 5. CMTS Board USB Mini-B Connector (J7)

Two MMPX connectors to output compliance mode toggle signal. These signals should be routed to the PER0 MMPX differential connectors of the CLB or CBB that the users DUT is connected to.

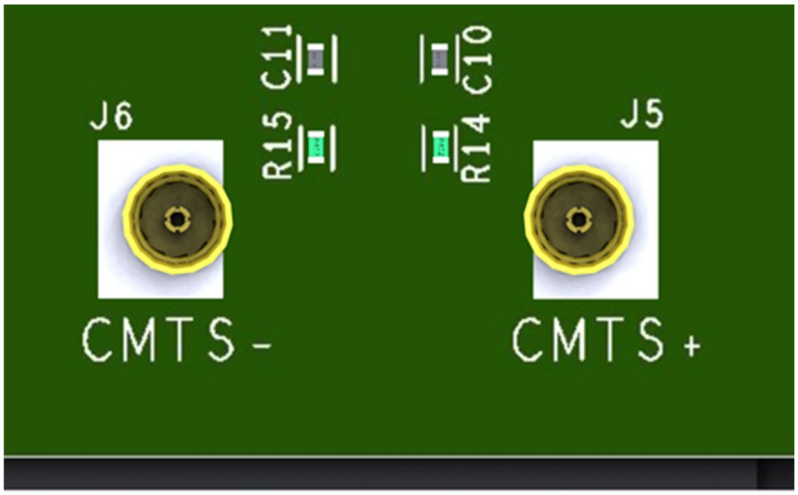


Figure 6. CMTS Differential Output SMP Connectors (J6 and J5)

CMTS push button. This button is used to generate the compliance mode toggle signal.

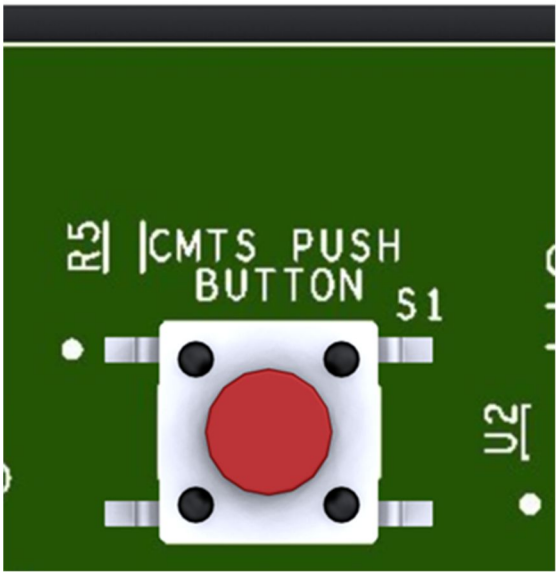


Figure 7. CMTS Push Button (S1)

The CMTS automation header shown below can be used as an alternative to the CMTS push button to generates the compliance mode toggle signal. This header can be connected to a user interface (such as a standard GPIO) to control the compliance mode toggle signal.

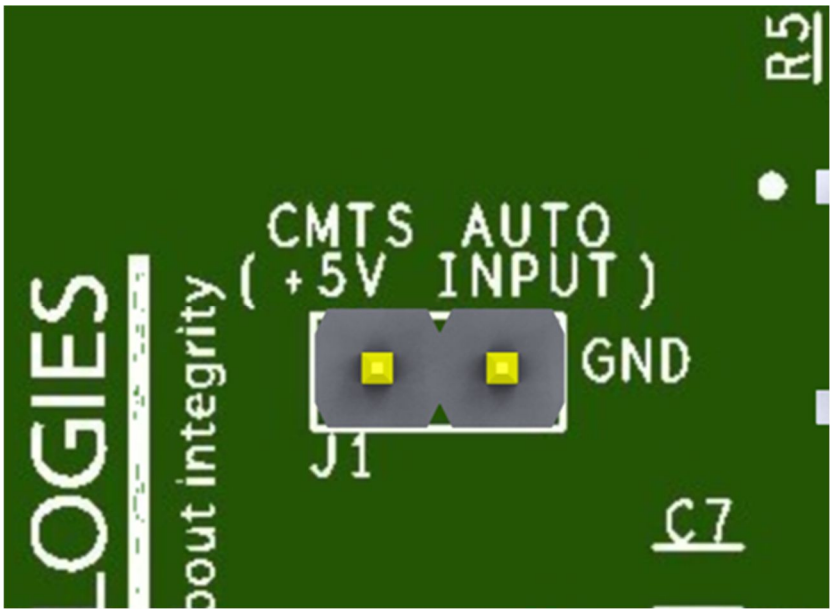


Figure 8. CMTS Automation Header (J1)

## CBB Test Fixture Features

- ATX Power Connector and Power Switch
    - The U.2 CBB uses a 24 pin ATX power connector. In addition, the on-board power switch enables power to be delivered to the CBB and DUT from the power supply when the switch is in the “ON” position.

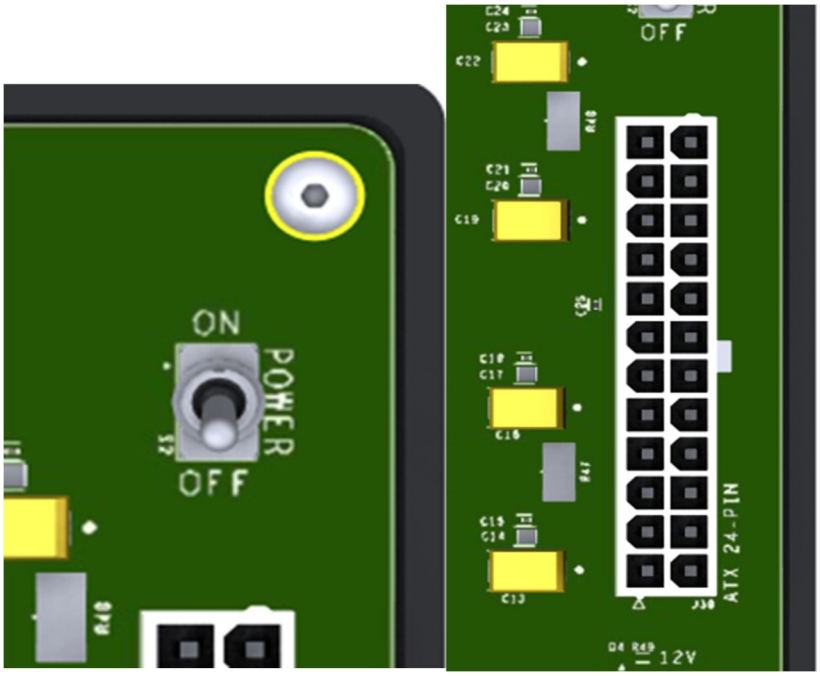


Figure 9. CBB Power Switch (S2) and 24-Pin ATX Power Connector (J30)

- REFCLK/SSC
  - The U.2 CBB can provide a REFCLK with no SSC, or two SSC settings of 0.25% downspread or 0.5% downspread. This selection is made using the REFCLK SSC selection switch. With the switch placed in the middle position, the U.2 CBB will provide a 100 MHz REFCLK with no SSC. Placing the switch in the "SSC ON -0.5%" position will enable 0.5% downspread SSC to the REFCLK and placing the switch in the "SSC ON -0.25%" position will enable 0.25% downspread to the REFCLK. These SSC settings do not apply to an externally provided REFCLK and only to the REFCLK provided by the U.2 CBB fixture.

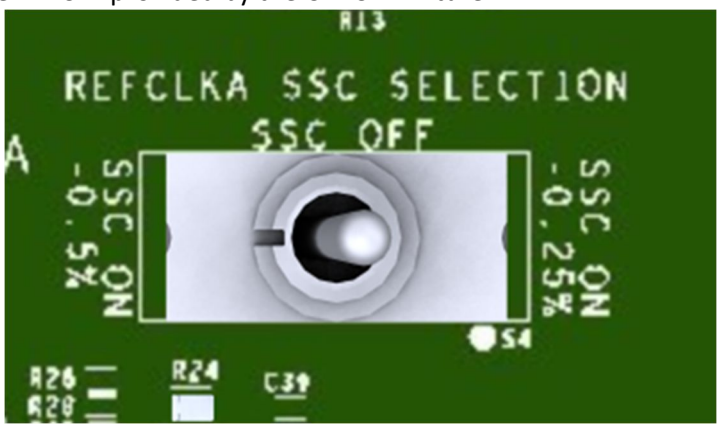


Figure 10. CBB REFCLK SSC Selection Switch (S4)

- REFCLK selection switch
  - The REFCLK allows the user to select between the REFCLK generated by the U.2 CBB or an externally provided REFCLK. When selecting an external REFCLK, this clock shall be provided to the U.2 CBB via the 2 "External REFCLK" SMP connectors.

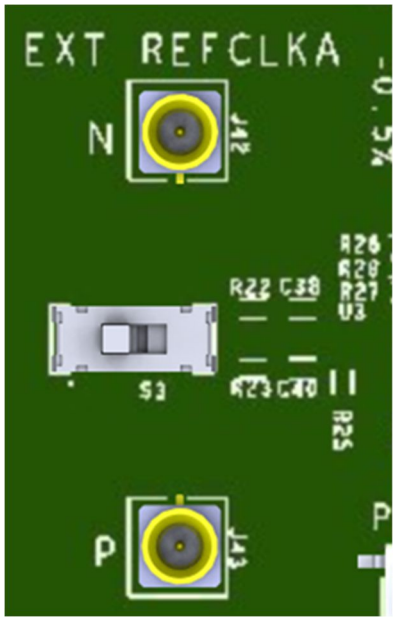


Figure 11. CBB REFCLK Selection Switch (S3)

- Dual port enable switch

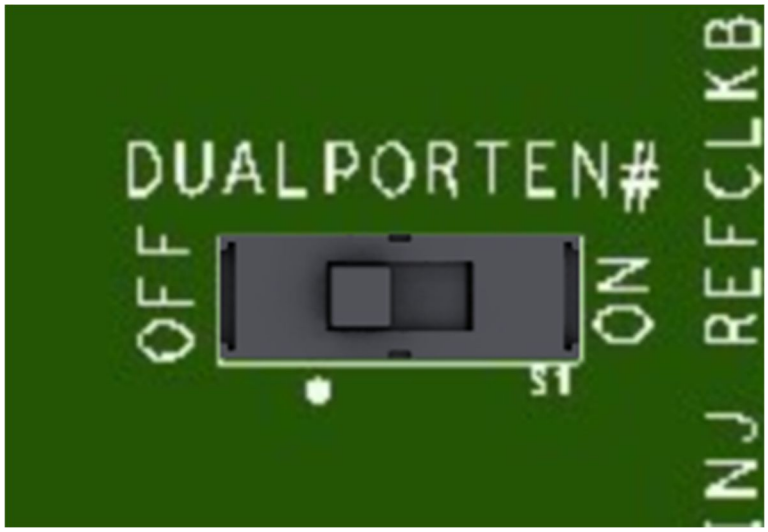


Figure 22. CBB Dual Port Enable Switch (S1)

  - The U.2 CBB features a DUALPORTEN# switch to enable Dual Port Mode. When this switch is in the off position, dual port is not enabled. When this switch is in the on position, dual port is enabled.

- PERST

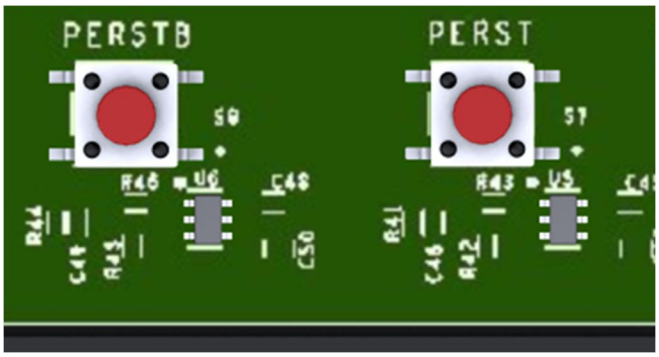


Figure 13. CBB PERST Push Buttons (S7 and S8)

  - The U.2 CBB supports up to two PERST (PCIe Reset) signals. PERST is the primary reset signal used to reset the DUT when dual port mode is not enabled or reset first A-side port when dual port is enabled. PERSTB is the second B-side port reset when dual port mode is enabled. These PERST signals will be low while there is no power applied to the U.2 CBB. Upon power up, the PERST signals will automatically go high after a 100 ms delay from when the last power rail on the U.2 CBB goes high to ensure all power rails at stable before de-asserting reset.


Figure 14. Automatic PERST Signal Delay (100 ms)

Additionally, the PERST push buttons can be used to manually trigger a 100 ms PERST signal to reset the DUT.

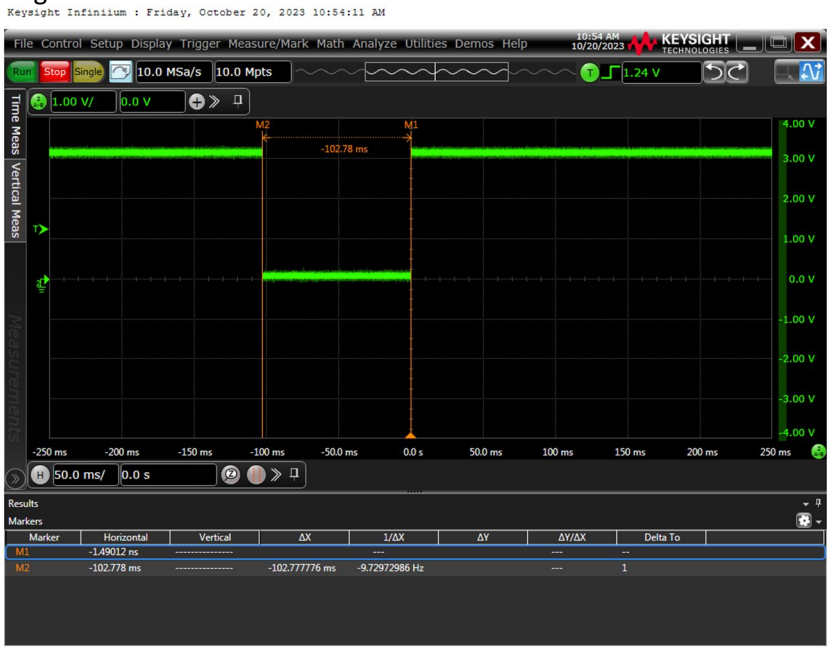


Figure 15. Manual PERST Signal (100 ms)

- Lane characterization
    - Lane characterization traces are included on both U.2 CLB and CBB fixtures. These characterization lanes include a short trace and long trace used to determine the loss per inch of the fixture being characterized. This is done by taking a through measurement of the short trace and a through measurement of the long trace. The difference in loss between the long and short trace divided by difference in length of the long trace and short trace will give the loss per inch of the fixture. The lengths of the long and short traces are listed below for the CLB and CBB fixtures:
        - Long Trace Length: 4”
        - Short Trace Length: 1”

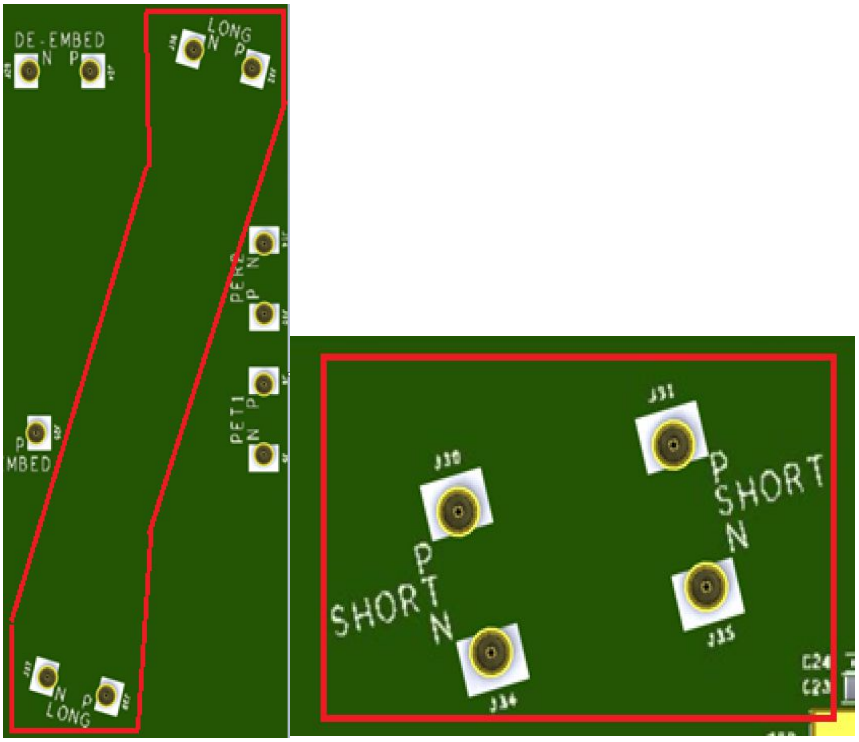


Figure 16. CBB Long and Short Characterization Channels

- In addition to the short and long traces, the 2x through channel and de-embed channels can be used to characterize the specific traces on the CBB or CLB. The de-embed channel is a replica of the 3" TX and RX traces on the CBB plus half of the 2X through. Therefore, by de-embedding half of the 2X through channel from the de-embed channel the TX and RX channels minus connector pads can be characterized.

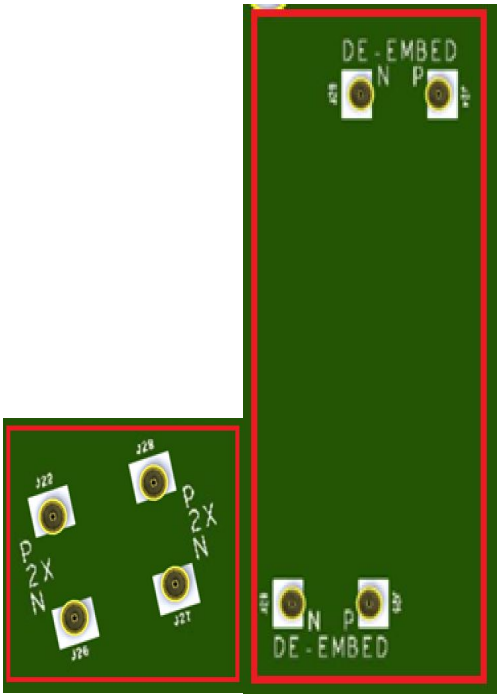


Figure 37. CBB 2X Thru and De-embed Channels

## CLB Test Fixture Features

- Lane characterization
    - Similarly to the CBB, the CLB also has a 2X through trace, short trace, and long trace. However, the short and long trace also serve as the de-embed traces for the RX traces (long trace) and TX traces (short trace).
        - Long Trace Length: 2.83”
        - Short Trace Length: 1.83”

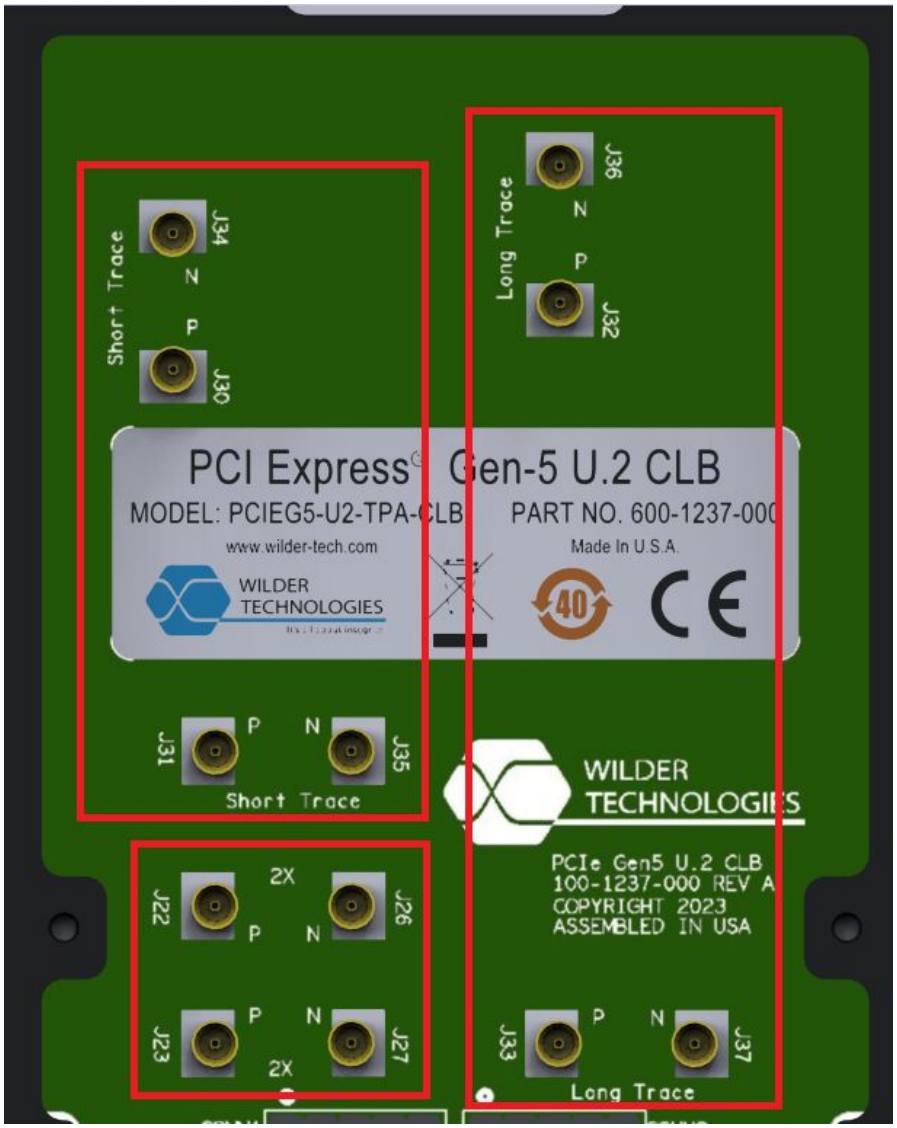


Figure 18. CLB Characterization Traces

- REFCLK SMP Connectors
  - The CLB has two differential SMP connectors for probing the REFCLK. The first set of differential SMP connectors (J18 and J19) are for REFCLKA and the second set of differential SMP connectors (J20 and J21) are for REFCLKB.

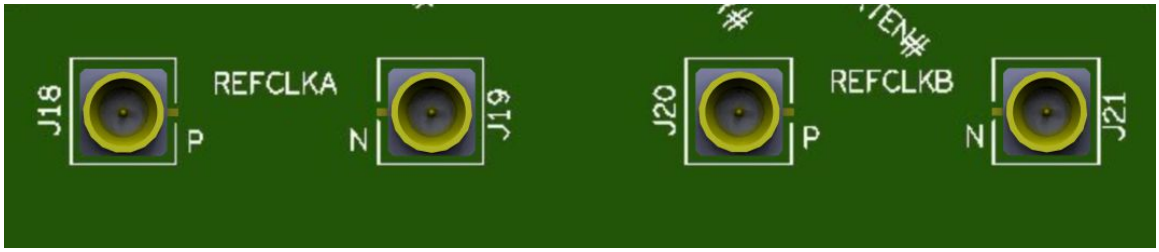


Figure 19. CBB REFCLK SMP Connectors

- Low Speed Header Pins
  - The CLB also has low speed header pins to connect to certain low speed signals from the system DUT.

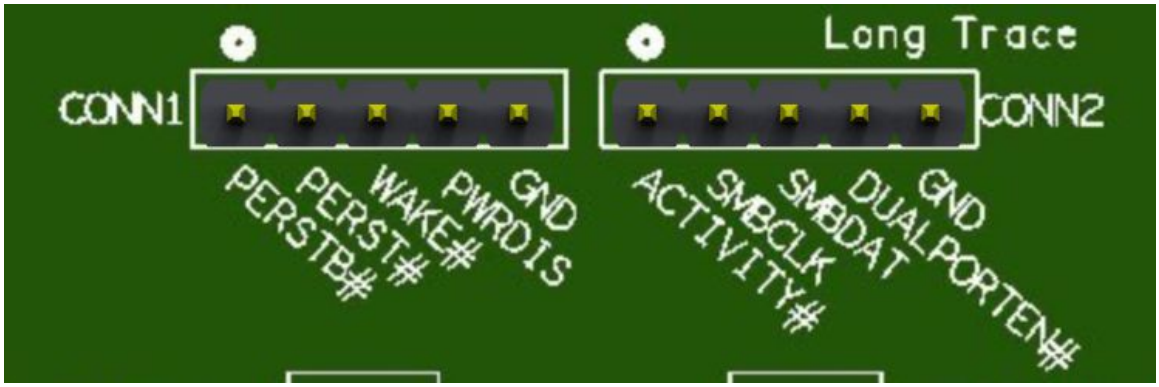


Figure 20. CLB Low Speed Header Pins

## TX Testing User Models

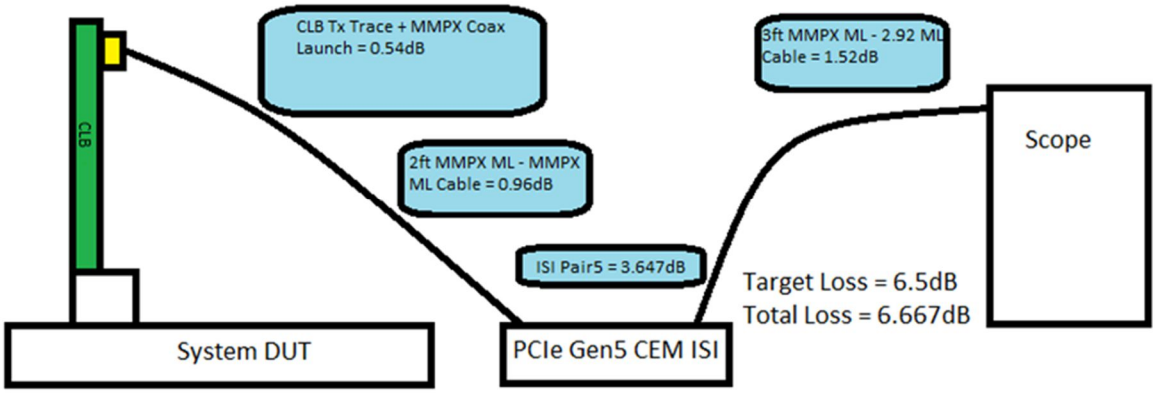


Figure 21. Total Test Channel Loss for Gen-5 Example

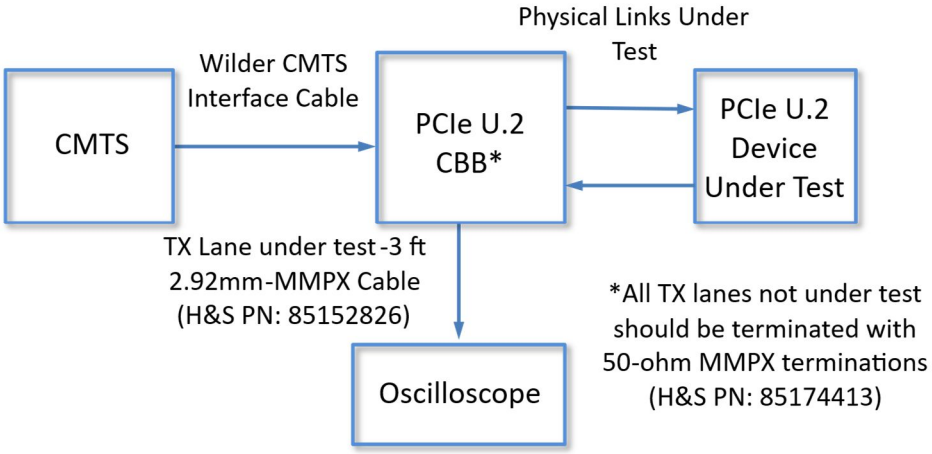


Figure 22. Device TX Test Setup Example

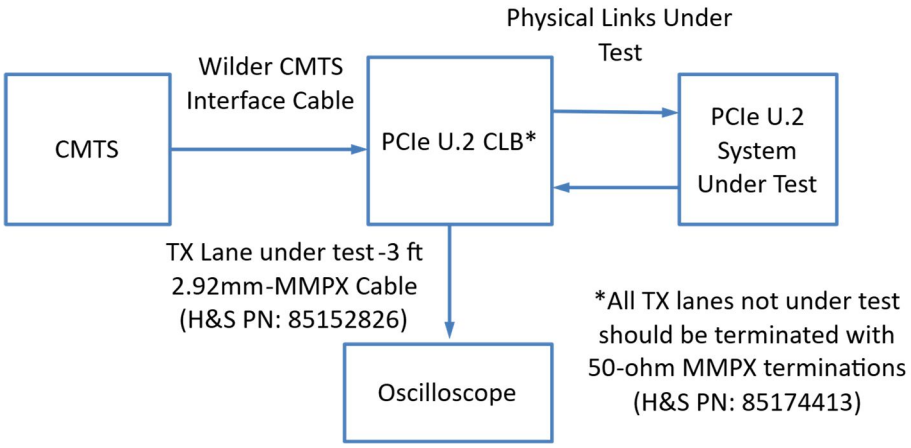


Figure 23. System Board TX Test Setup Example

## RX Testing User Models

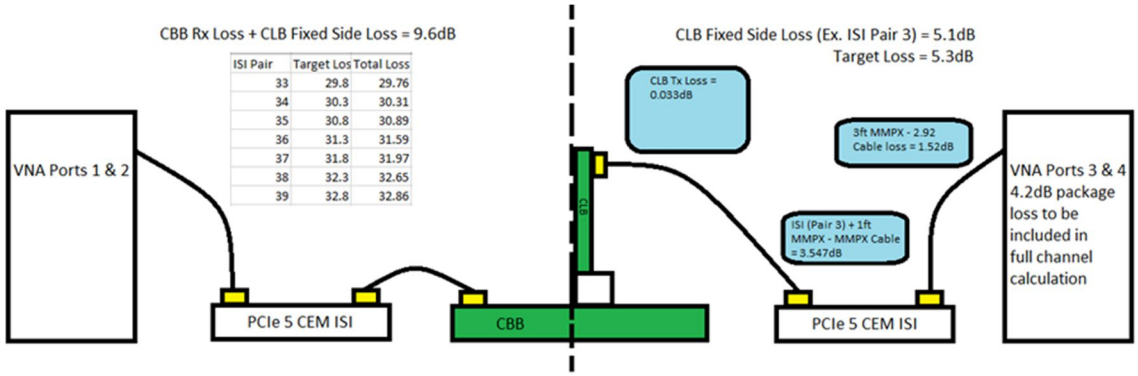


Figure 24. Device RX Calibration Example

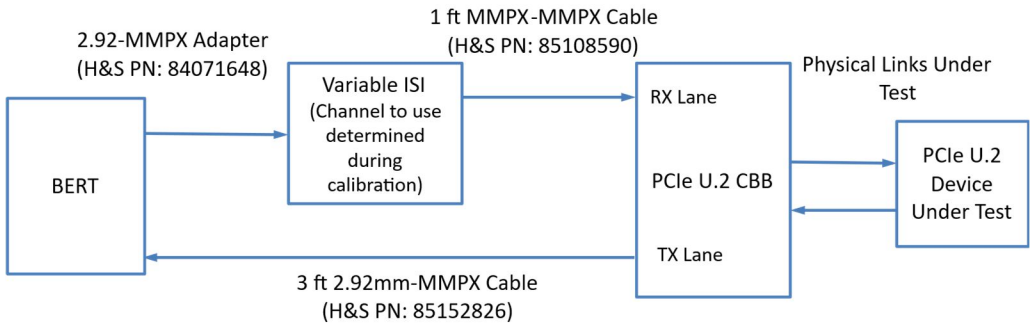


Figure 25. Device RX Test Setup Example

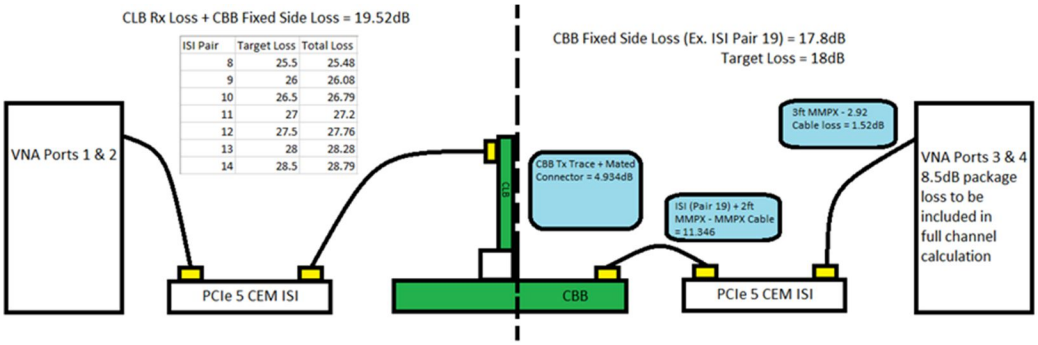


Figure 26. System RX Calibration Example

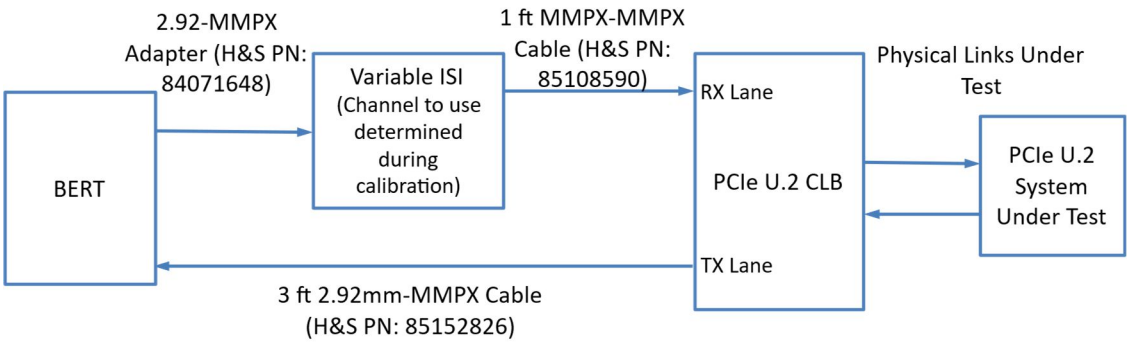


Figure 27. System RX Test Setup Example

# Mechanical and Environmental Specifications

**NOTE: All specifications in this manual are subject to change.**

**Table 3. General Specifications**

| ITEM | DESCRIPTION |
|---|---|
| Usage Environment | Controlled indoor environment |
| PCIEG5-U2-TPA-CLB (L x W x H) | 7.25” x 2.75” x 0.374” (184.2 mm x 69.9 mm x 9.5 mm) |
| PCIEG5-U2-TPA-CBB | 9.50” x 5.00” x 1.50” (241.3 mm x 127.0 mm x 38.1 mm) |
| PCIE-CMTS-TPA | 3.28” x 1.83” x 0.64” (83.3 mm x 46.5 mm x 16.3 mm) |
| Operating Temperature | 0°C to +55°C (32°F to +131°F) (Characteristic) |
| Storage Temperature | -40°C to +70°C (-40°F to +158°F) (Characteristic) |

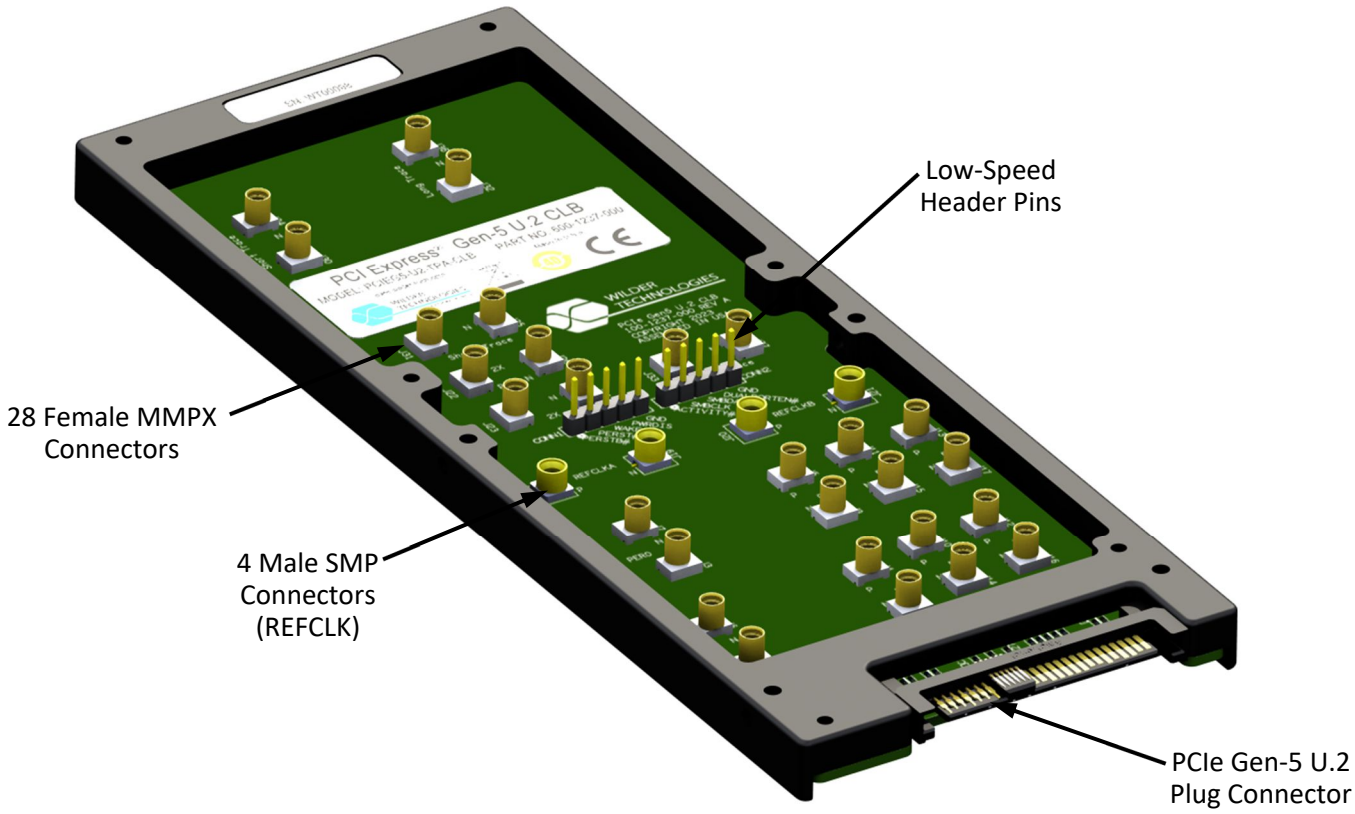


Figure 28. The PCIe Gen-5 U.2 Compliance Load Board (CLB)

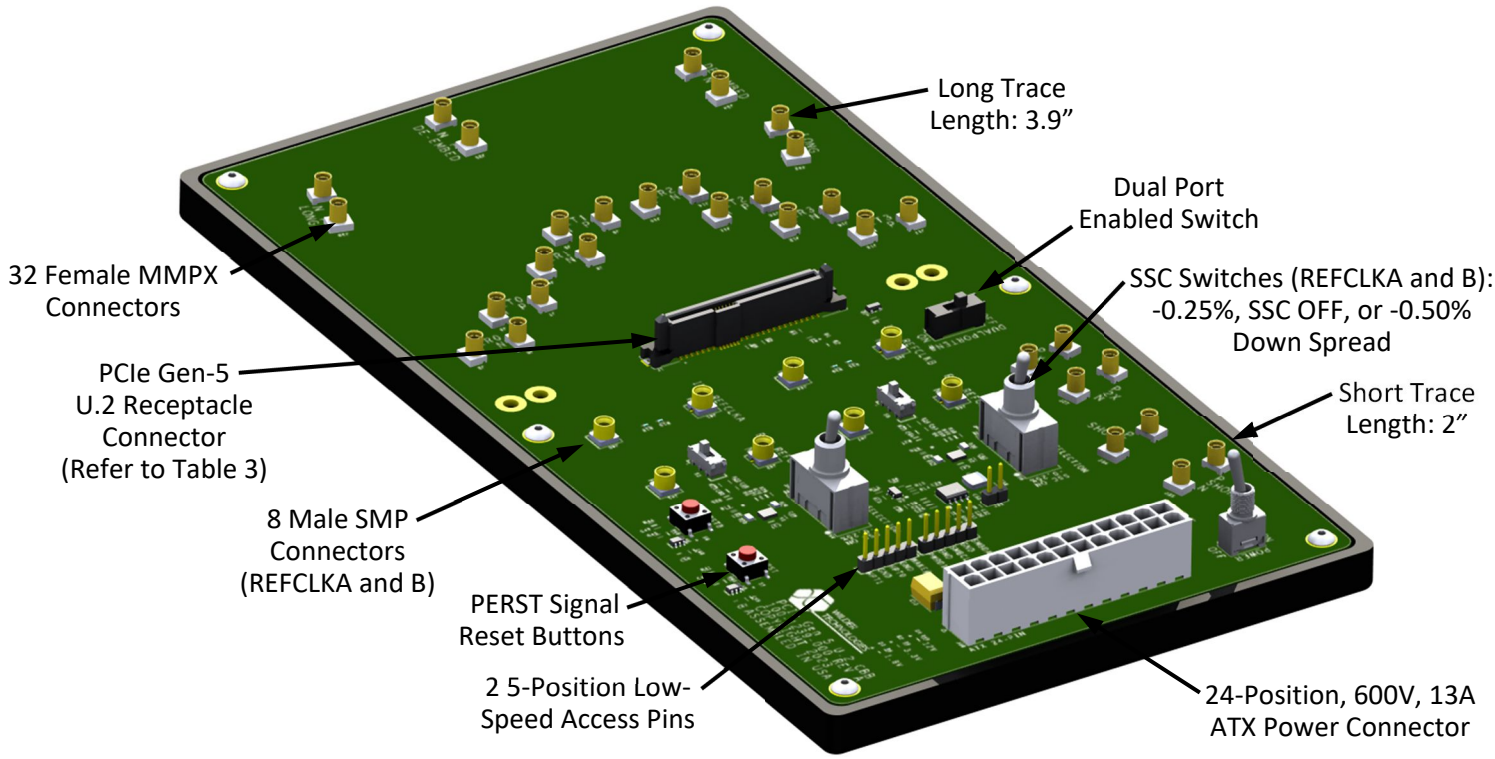


Figure 29. The PCIe Gen-5 U.2 Compliance Base Board (CBB)

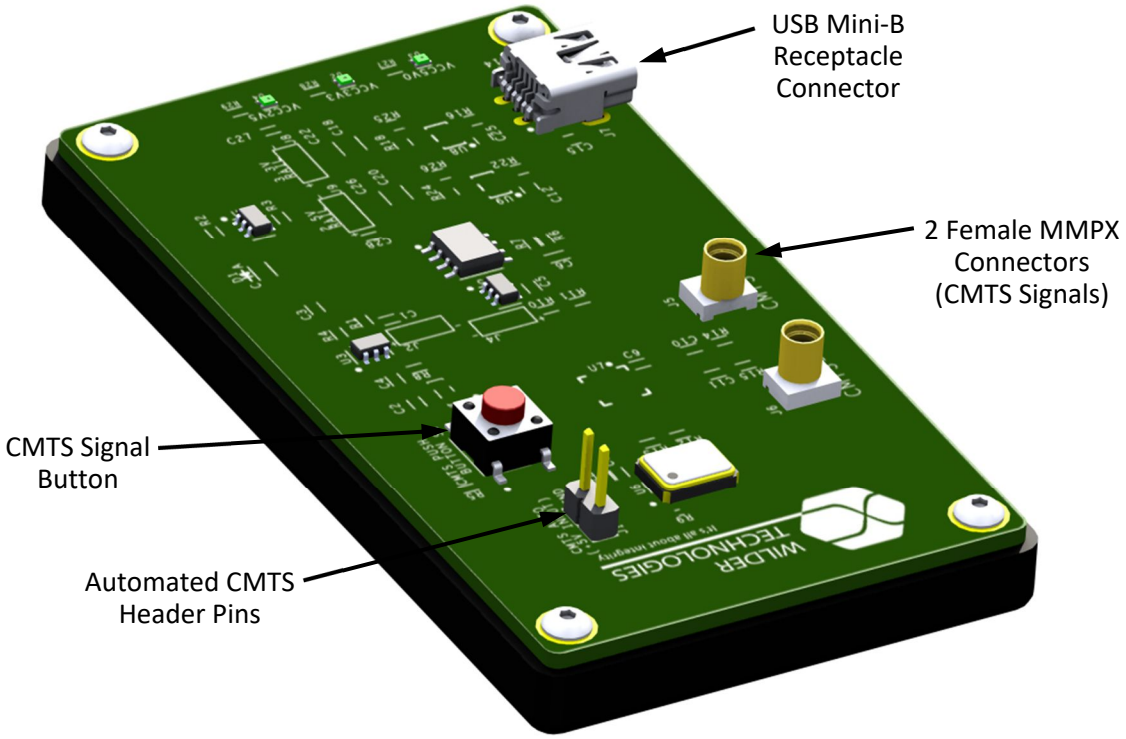


Figure 30. The PCIe Gen-5 Compliance Mode Toggle Signal (CMTS) Fixture

### Table 4. PCIe Gen-5 U.2 Receptacle (CBB) Pin Assignments

| Pin Description | Connector Pin Number | Device DUT Destination |
|---|---|---|
| Ground | P5, P6, P12, S1, S4, S7, S8, S11, S14, S16, S19, S22, S25, S28, E9, E12, E15, E19, E22 | GND |
| +12 V Pre-charge | P13 | +12 V Pre-charge |
| +12 V | P14, P15 | +12 V |
| +3.3 Vaux | E3 | +3.3 Vaux |
| No Connect | P2, P7, P8, P9, S2, S3, S5, S6, S9, S10, S12, S13, E6 | NC |
| PERp1 (PCIe RX Lane 1 Positive) | S17 | PERp1 |
| PERn1 (PCIe RX Lane 1 Negative) | S18 | PERn1 |
| PETn1 (PCIe TX Lane 1 Negative) | S20 | PETn1 |
| PETp1 (PCIe TX Lane 1 Positive) | S21 | PETp1 |
| PERp2 (PCIe RX Lane 2 Positive) | S23 | PERp2 |
| PERn2 (PCIe RX Lane 2 Negative) | S24 | PERn2 |
| PETn2 (PCIe TX Lane 2 Negative) | S26 | PETn2 |
| PETp2 (PCIe TX Lane 2 Positive) | S27 | PETp2 |
| PERp0 (PCIe RX Lane 0 Positive) | E10 | PERp0 |
| PERn0 (PCIe RX Lane 0 Negative) | E11 | PERn0 |
| PETn0 (PCIe TX Lane 0 Negative) | E13 | PETn0 |
| PETp0 (PCIe TX Lane 0 Positive) | E14 | PETp0 |
| PERp3 (PCIe RX Lane 3 Positive) | E17 | PERp3 |
| PERn3 (PCIe RX Lane 3 Negative) | E18 | PERn3 |
| PETn3 (PCIe TX Lane 3 Negative) | E20 | PETn3 |
| PETp3 (PCIe TX Lane 3 Positive) | E21 | PETp3 |
| WAKE# (Wake) | P1 | WAKE# |
| PWRDIS (Power Disable) | P3 | PWRDIS |
| IfDet# (Interface Type Detection) | P4 | IfDet# |
| PRSNT# (Presence Detect) | P10 | PRSNT# |
| ACTIVITY# (Activity Indicator) | P11 | ACTIVITY# |
| HPT0 (Host Port Type-0) | S15 | HPT0 |
| REFCLKB+ (Reference clock for second B-side port if dual port mode is enabled) | E1 | REFCLKB+ |
| REFCLKB- (Reference clock for second B-side port if dual port mode is enabled) | E2 | REFCLKB- |
| CLKREQ# (Clock request, dual port not enabled) /PERSTB# (Reset for second B-side port) | E4 | CLKREQ#/PERSTB# |
| PERST# (Reset. If dual port mode is enabled, then first A-side port reset) | E5 | PERST# |
| REFCLK+ (Reference clock. First A-side port reference clock if dual port mode is enabled) | E7 | REFCLK+ |
| REFCLK- (Reference clock. First A-side port reference clock if dual port mode is enabled) | E8 | REFCLK- |
| HPT1 (Host Port Type-1) | E16 | HPT1 |
| SMBCLK (SMBus Clock) | E23 | SMBCLK |
| SMBDAT (SMBus Data) | E24 | SMBDAT |
| DUALPORTEN# (Dual port Enable and Host Port Type Control) | E25 | DUALPORTEN# |

### Table 5. PCIe Gen-5 U.2 Plug (CLB) Pin Assignments

| Pin Description | Connector Pin Number | System DUT Destination |
|---|---|---|
| Ground | P5, P6, P12, S1, S4, S7, S8, S11, S14, S16, S19, S22, S25, S28, E9, E12, E15, E19, E22 | GND |
| +12 V Precharge | P13 | +12 V Precharge |
| +12 V | P14, P15 | +12 V |
| +3.3 Vaux | E3 | +3.3 Vaux |
| No Connect | P2, P7, P8, P9, S2, S3, S5, S6, S9, S10, S12, S13, E6 | NC |
| PETp1 (PCIe TX Lane 1 Positive) | S17 | PETp1 |
| PETn1 (PCIe TX Lane 1 Negative) | S18 | PETn1 |
| PERn1 (PCIe RX Lane 1 Negative) | S20 | PERn1 |
| PERp1 (PCIe RX Lane 1 Positive) | S21 | PERp1 |
| PETp2 (PCIe TX Lane 2 Positive) | S23 | PETp2 |
| PETn2 (PCIe TX Lane 2 Negative) | S24 | PETn2 |
| PERn2 (PCIe RX Lane 2 Negative) | S26 | PERn2 |
| PERp2 (PCIe RX Lane 2 Positive) | S27 | PERp2 |
| PETp0 (PCIe TX Lane 0 Positive) | E10 | PETp0 |
| PETn0 (PCIe TX Lane 0 Negative) | E11 | PETn0 |
| PERn0 (PCIe RX Lane 0 Negative) | E13 | PERn0 |
| PERp0 (PCIe RX Lane 0 Positive) | E14 | PERp0 |
| PETp3 (PCIe TX Lane 3 Positive) | E17 | PETp3 |
| PETn3 (PCIe TX Lane 3 Negative) | E18 | PETn3 |
| PERn3 (PCIe RX Lane 3 Negative) | E20 | PERn3 |
| PERp3 (PCIe RX Lane 3 Positive) | E21 | PERp3 |
| WAKE# (Wake) | P1 | WAKE# |
| PWRDIS (Power Disable) | P3 | PWRDIS |
| IfDet# (Interface Type Detection) | P4 | IfDet# |
| PRSNT# (Presence Detect) | P10 | PRSNT# |
| ACTIVITY# (Activity Indicator) | P11 | ACTIVITY# |
| HPT0 (Host Port Type-0) | S15 | HPT0 |
| REFCLKB+ (Reference clock for second B-side port if dual port mode is enabled) | E1 | REFCLKB+ |
| REFCLKB- (Reference clock for second B-side port if dual port mode is enabled) | E2 | REFCLKB- |
| CLKREQ# (Clock request, dual port not enabled) /PERSTB# (Reset for second B-side port) | E4 | CLKREQ#/PERSTB# |
| PERST# (Reset. If dual port mode is enabled then first A-side port reset) | E5 | PERST# |
| REFCLK+ (Reference clock. First A-side port reference clock if dual port mode is enabled) | E7 | REFCLK+ |
| REFCLK- (Reference clock. First A-side port reference clock if dual port mode is enabled) | E8 | REFCLK- |
| HPT1 (Host Port Type-1) | E16 | HPT1 |
| SMBCLK (SMBus Clock) | E23 | SMBCLK |
| SMBDAT (SMBus Data) | E24 | SMBDAT |
| DUALPORTEN# (Dual port Enable and Host Port Type Control) | E25 | DUALPORTEN# |

# Electrical Specifications

**NOTE: All specifications in this manual are subject to change.**

**Table 6. Electrical Specifications**

| SPECIFICATION | TYPICAL | NOTES |
|---|---|---|
| Differential Impedance (ohms), 100 ps Rise Time | 85 ± 5% | All Differential Pairs, CBB and CLB, excluding PCIe U.2 connector. |
| Differential Impedance (ohms), 100 ps Rise Time | 100 ± 5% | REFCLK Differential Pairs, CBB and CLB, excluding PCIe U.2 connector. |
| Impedance (ohms), 100 ps Rise Time | 42.5 ± 5% | All Single-Ended High-Speed Signals, CBB and CLB, excluding PCIe U.2 connector. |
| Impedance (ohms), 30 ps Rise Time | 50 ± 7% | MMPX Connectors |
| NEXT (dB), at 16 GHz | -40 | All Differential Pairs, single aggressor, with PCIe U.2 connector and terminations |
| Current Carrying (A) | 2.5 | +3.3V Power |

## Typical High-Speed Serial Characteristics

The high-speed serial measurements of the PCIe Gen-5 U.2 Test Adapters use a 4-port (50 Ω) VNA calibrated from 50 MHz to 40 GHz with 800 points. The measurements are in the form of S-parameters.

The S-parameter measurements are renormalized to 42.5 Ω ports instead of 50 Ω ports. This was done so that the port impedance and adapter impedance match.

In addition, 2.92 mm to MMPX adapters and MMPX connectors are included in the S-parameter measurements, but they are then gated out of the return loss due to their 50 Ω impedance.

Ultimately, this post-processing makes the S-parameters accurately represent the performance of the high-speed channels of only the U.2 adapters.

## Characterization (CLB and CBB Independent Only)

To characterize the real high-speed channels of the adapters only (no connector), the replica channels must be used. These replica channels include MMPX connector lead-in for what would be the U.2 connector side of the high-speed channels. This connector lead-in that is part of the S-parameter measurement must then be de-embedded to represent the real high-speed channels.

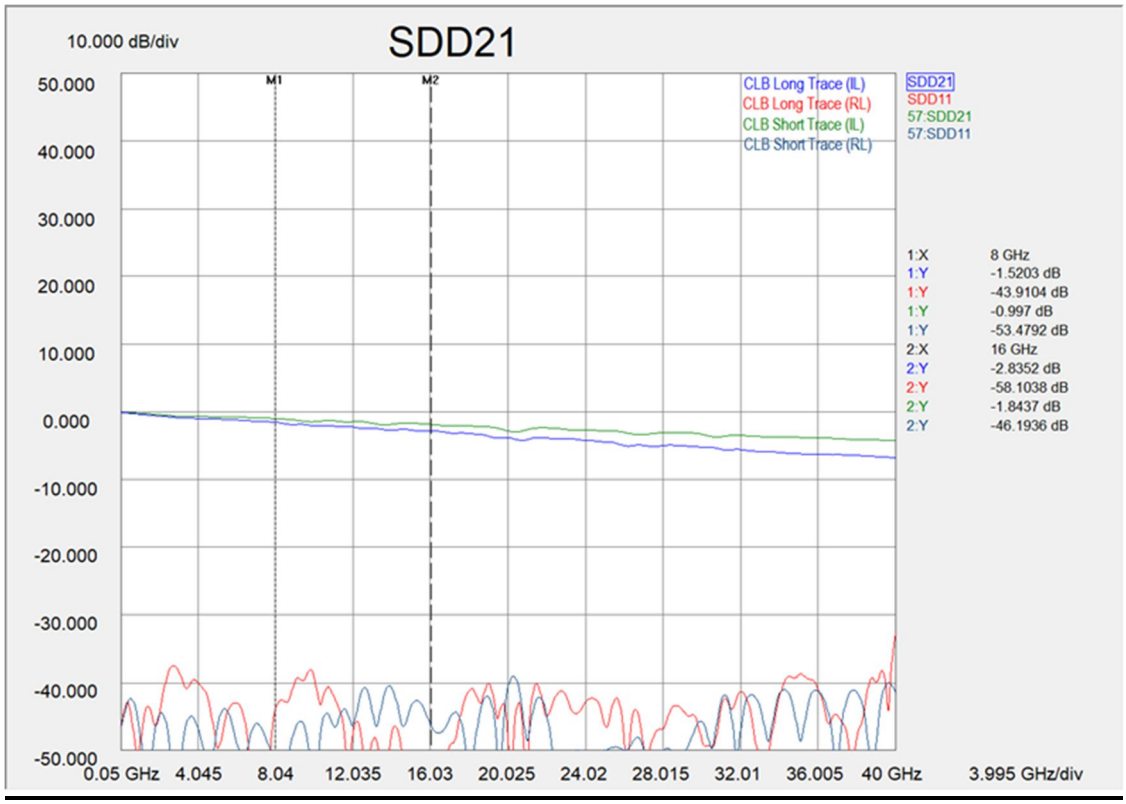


Figure 31. CLB (PCIEG5-U2-TPA-CLB) characterization with renormalization and gating

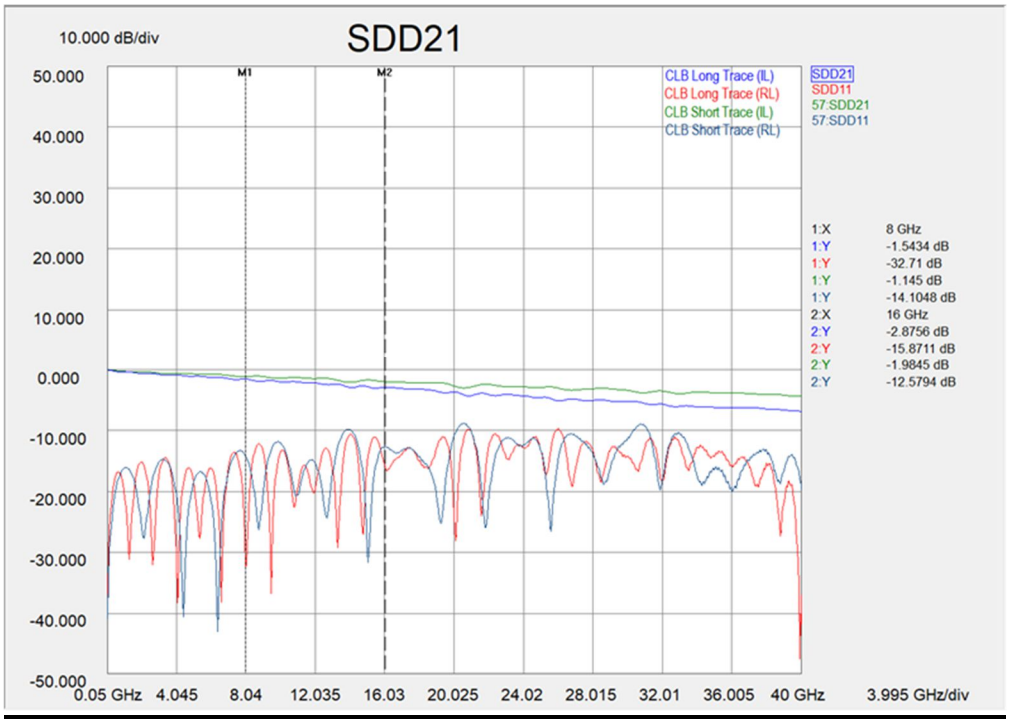


Figure 32. CLB (PCIEG5-U2-TPA-CLB) characterization without renormalization or gating

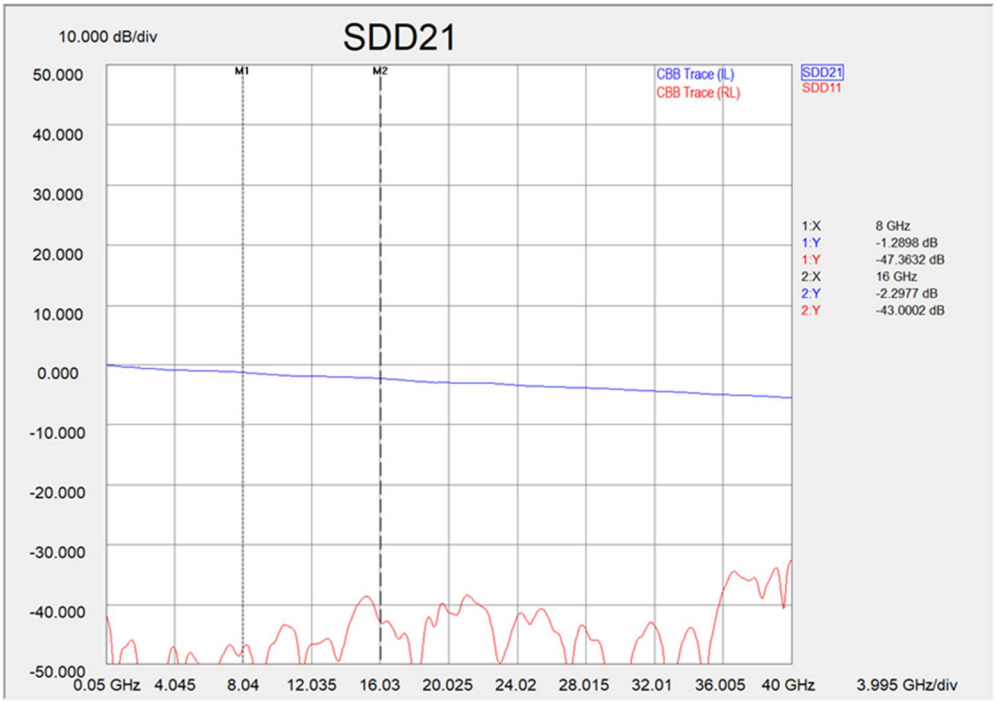


Figure 33. CBB (PCIEG5-U2-TPA-CBB) characterization with renormalization and gating

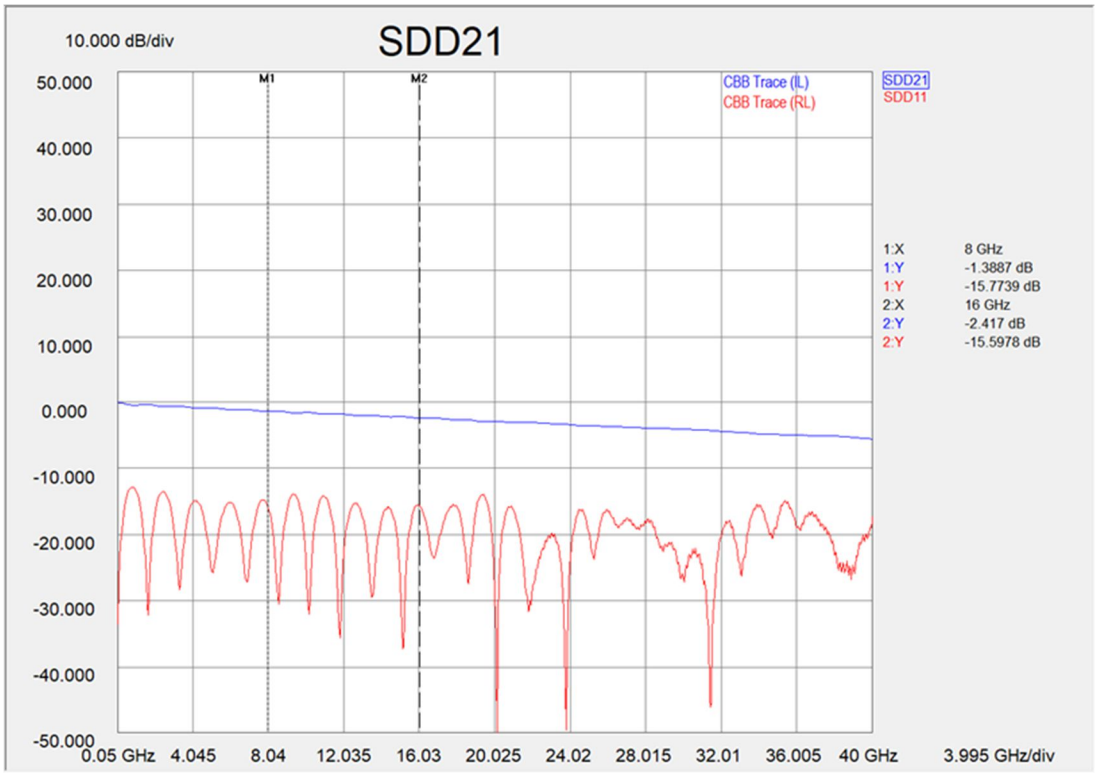


Figure 34. CBB (PCIEG5-U2-TPA-CBB) characterization without renormalization or gating

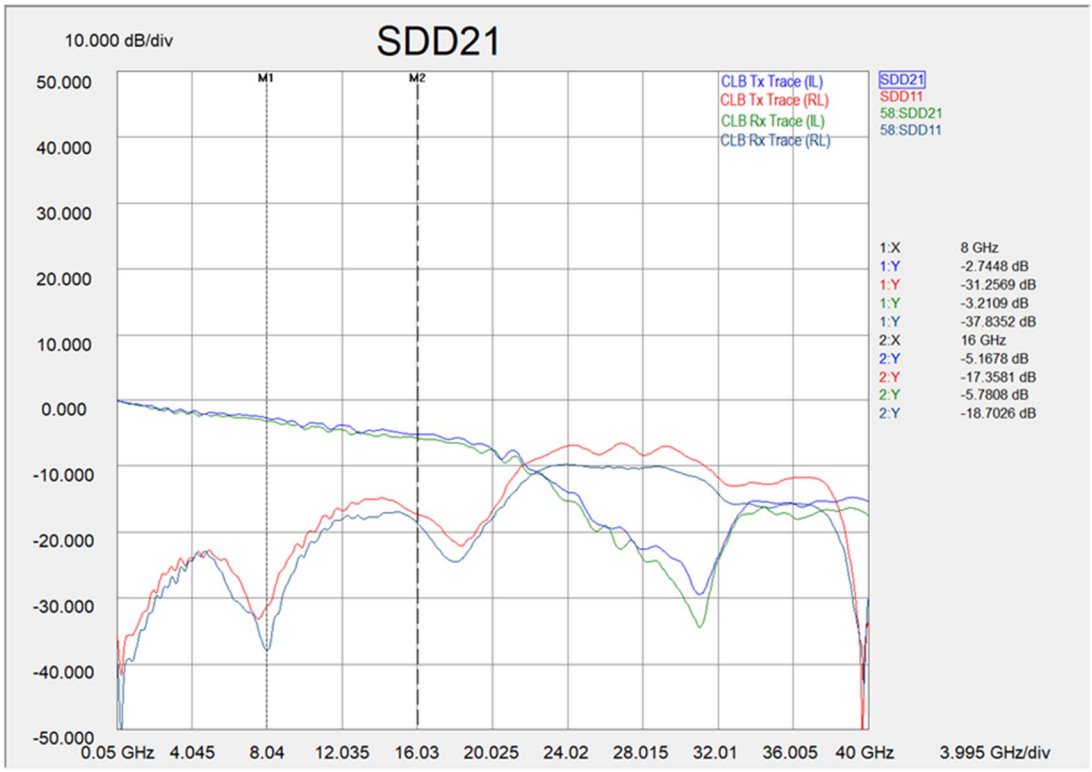


Figure 35. CLB and CBB (PCIEG5-U2-TPA-CLBCBB) mated insertion and return loss with renormalization and gating

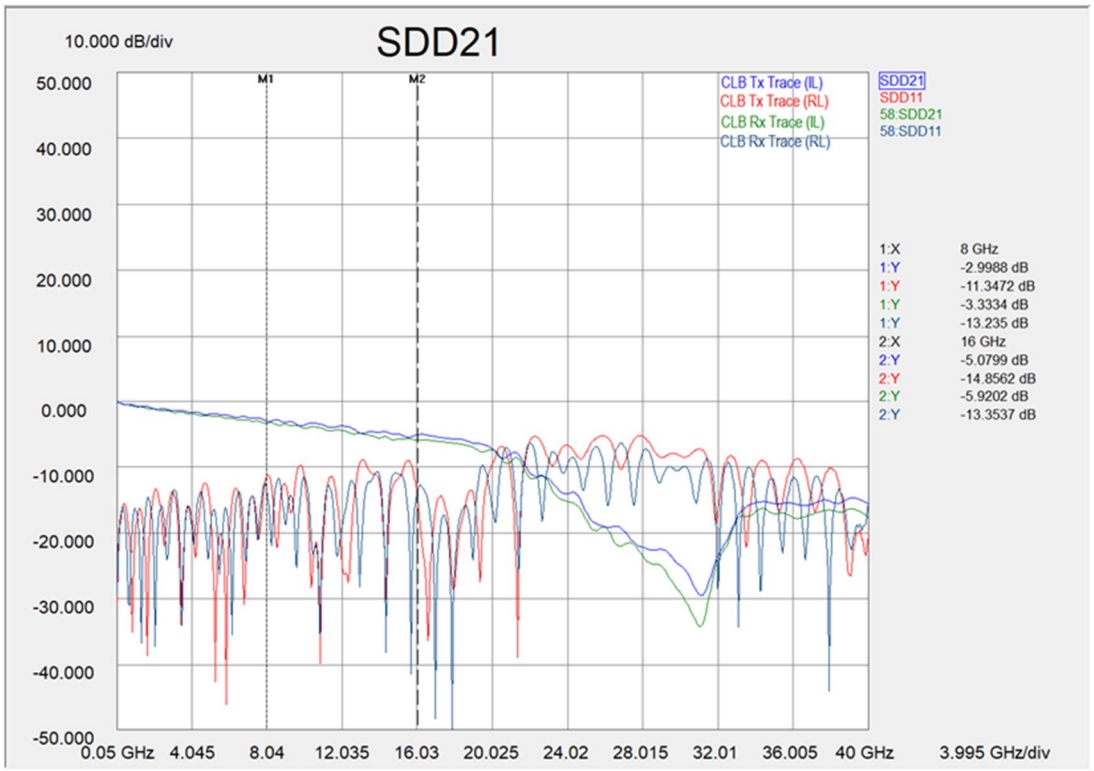


Figure 36. CLB and CBB (PCIEG5-U2-TPA-CLBCBB) mated insertion and return loss without renormalization or gating

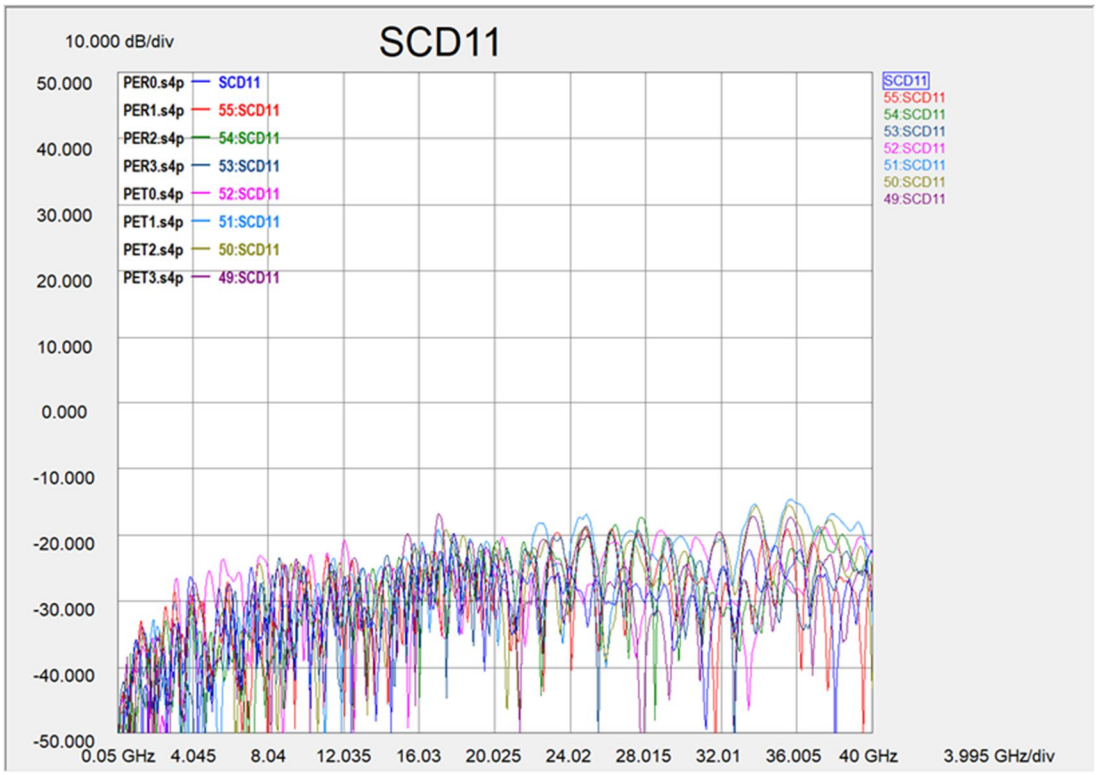


Figure 37. CLB and CBB (PCIEG5-U2-TPA-CLBCBB) mated conversion loss

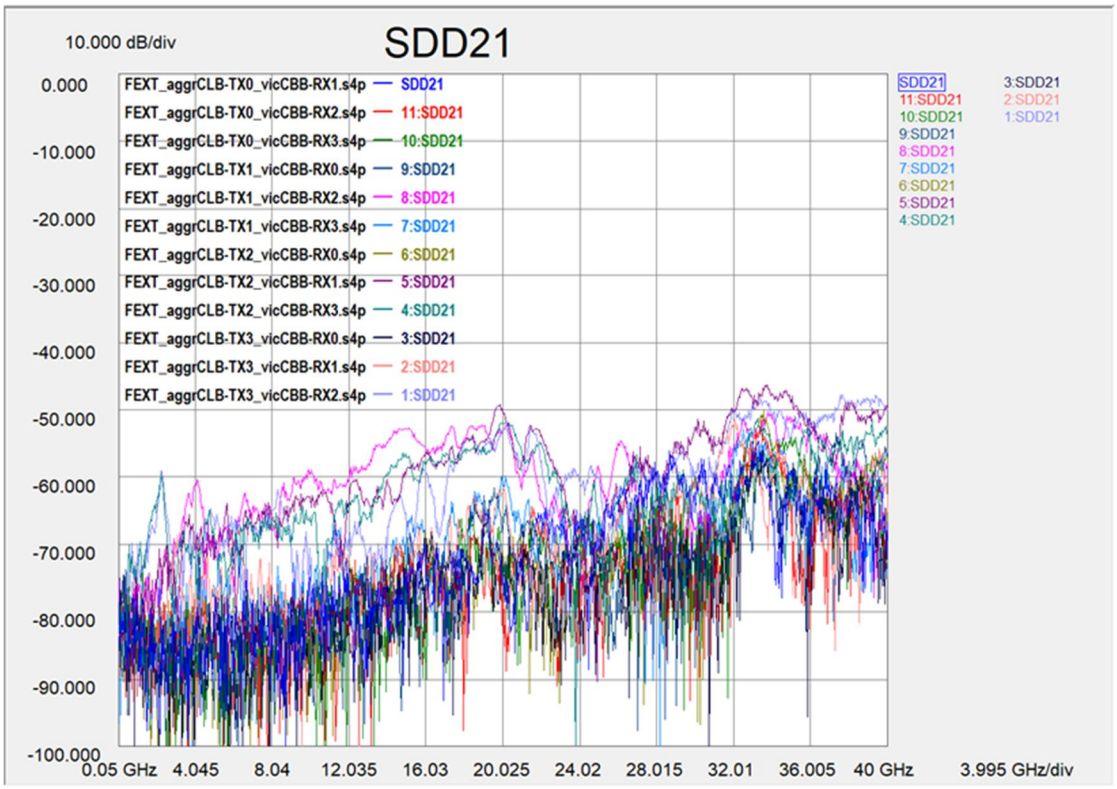


Figure 38. CLB and CBB (PCIEG5-U2-TPA-CLBCBB) mated FEXT

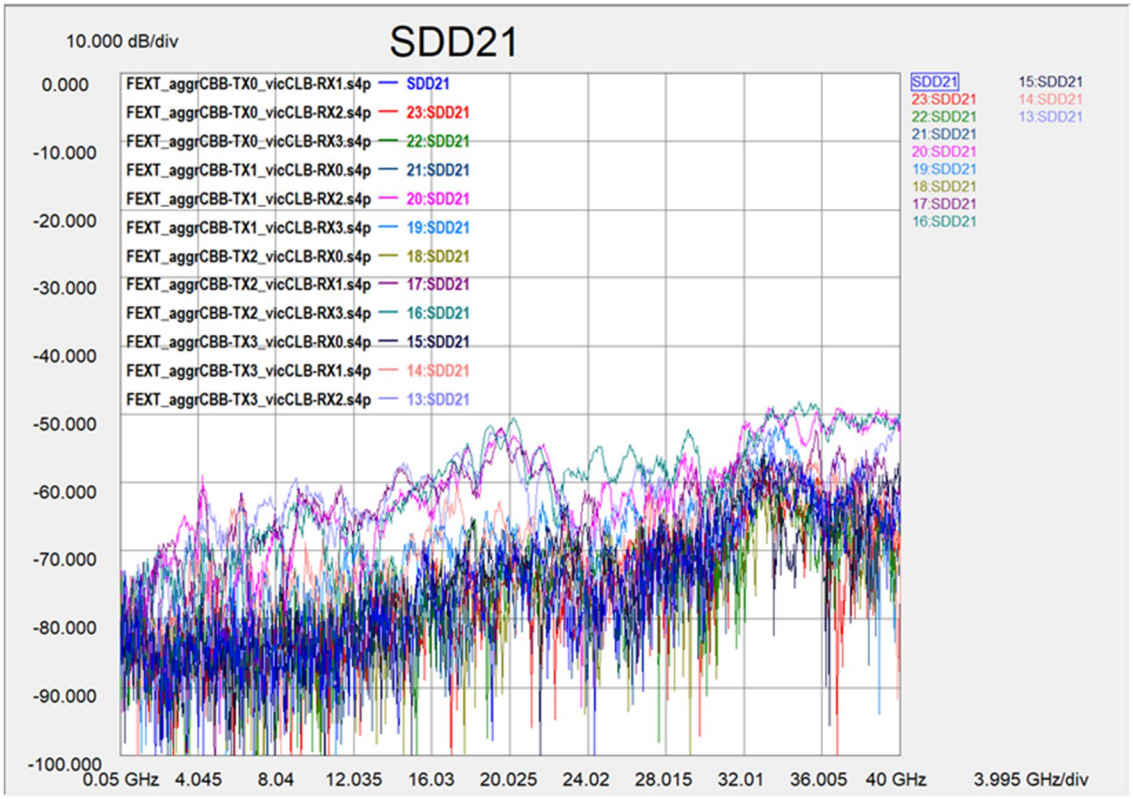


Figure 39. CLB and CBB (PCIEG5-U2-TPA-CLBCBB) mated NEXT

# Compliance with Environmental Legislation

Wilder Technologies, LLC, is dedicated to complying with the requirements of all applicable environmental legislation and regulations, including appropriate recycling and/or disposal of our products.

## WEEE Compliance Statement

The European Union adopted Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE), with requirements that went into effect August 13, 2005. WEEE is intended to reduce the disposal of waste from electrical and electronic equipment by establishing guidelines for prevention, reuse, recycling and recovery.

Wilder Technologies has practices and processes in place to conform to the requirements in this important Directive.

In support of our environmental goals, effective January 1st, 2009 Wilder Technologies, LLC has partnered with EG Metals Inc. – Metal and Electronics Recycling of Hillsboro, Oregon, www.egmetalrecycling.com, to recycle our obsolete and electronic waste in accordance with the European Union Directive 2002/96/EC on waste electrical and electronic equipment ("WEEE Directive").

As a service to our customers, Wilder Technologies is also available for managing the proper recycling and/or disposal of all Wilder Technologies products that have reached the end of their useful life. For further information and return instructions, contact support@wilder-tech.com.

## Compliance To RoHS 2 Substance Restrictions

Wilder Technologies, LLC certifies that the parts described in this document are compliant to the substance restrictions of Directive 2011/65/EU of the European Parliament, and of the Council of 8 June, 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS 2 Directive), prohibiting the use in homogeneous materials in excess of the listed maximum concentration value, except in cases where use is allowed by applicable exemptions listed in Annex III and Annex IV of the Directive.

Compliance with RoHS 2 has been verified through internal controls at design and production sites, including establishment of processes for specifying and controlling materials and segregation of non-compliant parts, receipt of supplier declarations of compliance and/or analytical test.

# Glossary of Terms

| TERMINOLOGY | DEFINITION |
|---|---|
| Aggressor | A signal imposed on a system (i.e., cable assembly) to measure response on other signal carriers. |
| CEM | Card Electromechanical |
| Decibel (dB) | Ten times the common logarithm (i.e. log10) of the ratio of relative powers. |
| Informative | The designation of a test that is not required for compliance but is considered important from a characterization standpoint. It is provided for informational purposes only. |
| Insertion loss | The ratio, expressed in dB, of incident power to delivered power. |
| Far-end crosstalk (FEXT) | Crosstalk that is propagated in a disturbed channel in the same direction as the propagation of a signal in the aggressor channel. The terminals of the aggressor channel and the victim channel are usually close to each other. |
| PCIe | Peripheral Component Interconnect Express |
| PCIEG5-U2-TPA | PCIe Gen-5 U.2 Test Fixture. A specialized assembly that interfaces to an PCIe U.2 (SFF-8639) Receptacle or Plug and enables access of signals for measurement or stimulation. |
| U.2 | Formally called Small Form Factor 8639 (SFF-8639) |
| Near-end crosstalk (NEXT) | Crosstalk that is propagated in a disturbed channel in the opposite direction as the propagation of a signal in the aggressor channel. The terminals of the aggressor channel and the victim channel are usually close to each other. |
| Normative | The designation of a test that is required for compliance. |
| Return Loss | The ratio, expressed in dB, of incident power to reflected power. |
| RoHS | Restriction of Hazardous Substances Directive |
| USB | Universal Serial Bus |
| Victim | A signal carrier on a system that has a response imposed on it by other signals in the system. |

# Index

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